INTEGRATED CIRCUITS

LAB MANUAL

EEC-551

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CONTENTS

SYLLABUS INTEGRATED CIRCUITS

EEC 551 INTEGRATED CIRCUITS LAB

Objective: - To design and implement the circuits to gain knowledge on performance of the circuit and its application. These circuits should also be simulated on Pspice.

1. Log and antilog amplifiers.

2. Voltage comparator and zero crossing detectors.

3. Second order filters using operational amplifier for–
   a. Low pass filter of cutoff frequency 1 KHz.
   b. High pass filter of frequency 12 KHz.
   c. Band pass filter with unit gain of pass band from 1 KHz to 12 KHz.

4. Wien bridge oscillator using operational amplifier.

5. Determine capture range; lock in range and free running frequency of PLL.

6. Voltage regulator using operational amplifier to produce output of 12V with maximum load current of 50 mA.

7. A/D and D/A convertor.

8. Voltage to current and current to voltage convertors.

9. Function generator using operational amplifier (sine, triangular & square wave)

10. Astable and monostable multivibrator using IC 555.

Experiment Number-1

Design of Active Filters

Aim: To design and obtain the frequency response of second order Low Pass Filter (LPF)

APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	Resistor	33KΩ,27 kΩ,10 kΩ	2 ,1,1
2	Potentiometer	20k	1
3	Capacitor	0.0047 μF	2
4	I.C. 741 OP-AMP		1
	Function Generator	1MHz	1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

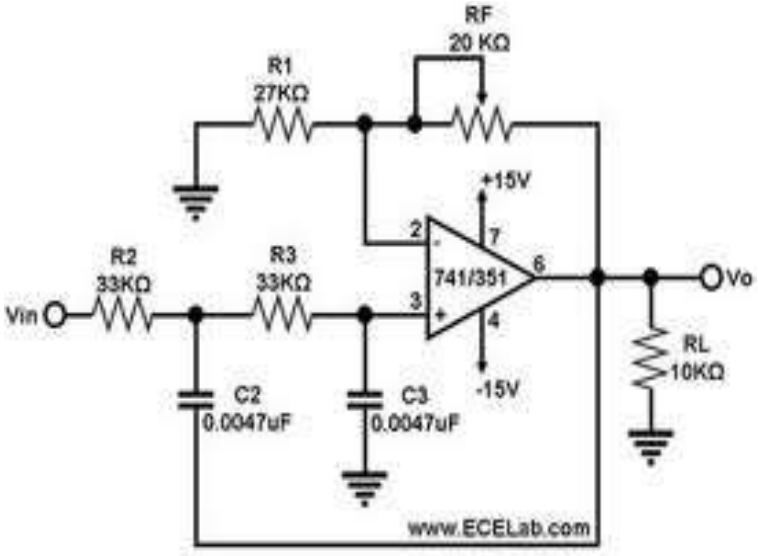
A LPF allows frequencies from 0 to higher cut of frequency, f_H. At f_H, the gain is 0.707 A_{max}, and after f_H gain decreases at a constant rate with an increase in frequency. The gain decreases 20dB each time the frequency is increased by 10. Hence the rate at which the gain rolls off after f_H is 20dB/decade or 6 dB/ octave, where octave signifies a two fold increase in frequency. The frequency f= f_H is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB from 0 Hz. Other equivalent terms for cut-off frequency are - 3dB frequency, break frequency, or corner frequency. The cutoff frequency is given as

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

For the sake of simplicity let us take $R_2 = R_3 = R$, $C_2 = C_3 = C$ then

$$f_H = \frac{1}{2\pi RC}$$

Circuit Diagram:



Design:

1. Let the cutoff frequency f_H = 1 kHz.
2. Let us take a capacitor of value 0.0047 μF.

So the value of R can be calculated as

$$R = \frac{1}{2\pi C f_H} = \frac{1}{2\pi * 47 * 10^{-10} * 1 * 10^3} = 33.86\ k\Omega$$

Now $R_F = 0.586\ R_1$

Let R_1 = 27 kΩ so R_F = 15.82 kΩ.

PROCEDURE:

1. Connect the circuit as shown in the figure.
2. Apply sinusoidal wave of constant amplitude at the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table.

Observation Table:

Input frequency, f (Hz)	**Gain magnitude, $\lvert v_o/v_i \rvert$**	**Magnitude (dB) = 20log$\lvert v_o/v_i \rvert$**

RESULT: The frequency response is drawn and is found similar to that of theoretical one.

VIVA QUESTIONS:

1. Define a filter. How are filters classifieds?
2. What is a pass band and a stop band for a filter?
3. What are the advantages of active over passive ones?
4. What is the Butterworth response?
5. List the most commonly used filters.

Experiment Number –2

Design of Active Filters

Aim: To design and obtain the frequency response of second order High Pass Filter (HPF)

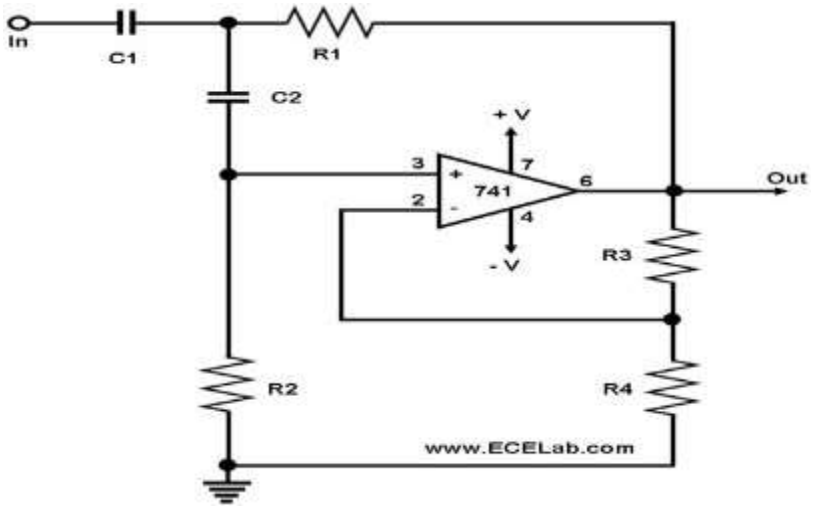
APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	Resistor	10KΩ	4
2	Potentiometer	20k,50k	1
3	Function Generator	1MHz	1
4	I.C. 741 OP-AMP		1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

The high pass filter can be obtained from the low pass by simply interchanging the frequency determining resistors and capacitors. The frequency at which the magnitude of the gain is 0.707 times the maximum value of gain is called lower cut off frequency. Obviously, all frequencies higher than f_L are pass band frequencies with the highest frequency determined by the closed loop band width of the op-amp.

Circuit Diagram:



Design:

3. Let the cutoff frequency f_L = 1 kHz.
4. Let us take a capacitor of value 0.0047 μF.

So the value of R can be calculated as

$$R = \frac{1}{2\pi C f_L} = \frac{1}{2\pi * 47 * 10^{-10} * 1 * 10^3} = 33.86\ k\Omega$$

Now $R_F = 0.586\ R_1$

Let R_1 = 27 kΩ so R_F = 15.82 kΩ.

PROCEDURE:

1. Connections are made as per the circuit diagrams shown in figure.
2. Apply sinusoidal wave of constant amplitude at the input such that op-amp does not go into saturation.
3. Vary the input frequency and note down the output amplitude at each step as shown in Table.

Observation Table:

Input frequency, f (Hz)	**Gain magnitude, $\lvert v_o/v_i \rvert$**	**Magnitude (dB) = 20log$\lvert v_o/v_i \rvert$**

RESULT: The frequency response is drawn and is found similar to that of theoretical one.

VIVA QUESTIONS:

6. Define a filter. How are filters classifieds?
7. What is a pass band and a stop band for a filter?
8. What are the advantages of active over passive ones?
9. What is the Butterworth response?
10. List the most commonly used filters.

Experiment Number- 3

Design of Log and Antilog Amplifier

AIM: To construct and study the behavior of logarithmic and antilogarithmic amplifier.

APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	Op-Amp 741 IC		1
2	Resistor	100 KΩ , 10 KΩ	2
3	NPN transistor BC 548		1
4	Function Generator	1MHz	1
5	CRO	20 MHz	1
6	Bread Board, Dc power supply		1
7	Connecting Wires and Probes		

THEORY:

The log and antilog amplifiers are the non linear application mode circuits. The grounded base NPN transistor behaves like a diode. Because the inverting terminal is on virtual ground the collector-base potential is zero and thereby it is behaving like a diode. So

$$I_E = I_S(e^{\frac{qV_E}{kT}} - 1)$$

Since $I_C = I_E$ for a grounded base transistor,

$$I_C = I_S\,(e^{\frac{qV_E}{kT}} - 1)$$

Where

I_S = emitter saturation current ≈ 10^{-13} A

k = Boltzmann's Constant

T = absolute temperature (in ^oK)

Therefore, $e^{\frac{qV_E}{kT}} = \frac{I_C}{I_S} + 1$

$$\approx \frac{I_C}{I_S}$$

Taking natural log on both sides, we get

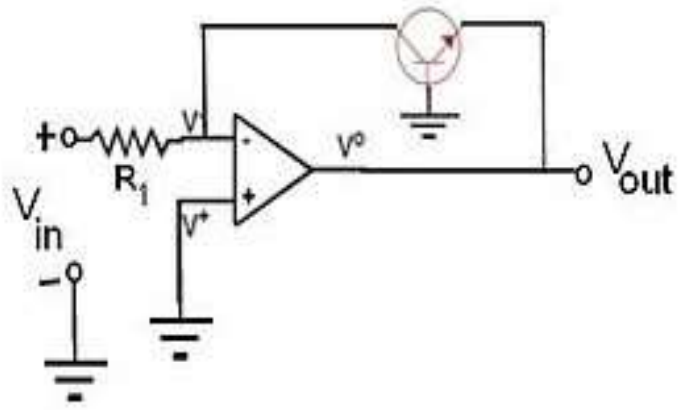
$V_E = \frac{kT}{q} \ln\left(\frac{I_c}{I_s}\right)$, also $V_E = -V_0$

$V_0 = -\frac{kT}{q} \ln\left(\frac{V_i}{I_S R_1}\right)$

Similarly for antilog amplifier

$$V_0 = -R_F I_S e^{(V_{in}/V_T)}$$

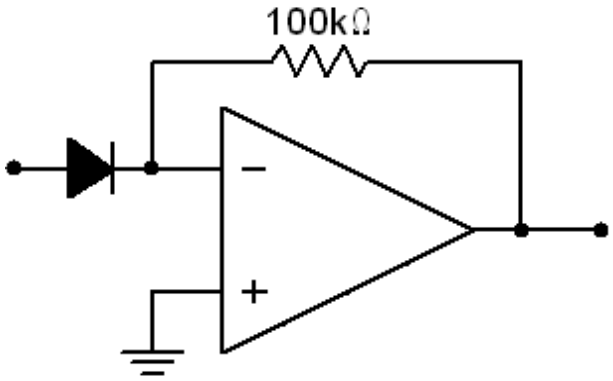
Circuit Diagram: (Log Amplifier)



Procedure:

1. Connect the circuit as shown in figure.
2. Set the input voltage to 1V.
3. See the voltage across the output terminal. Note the negative sign.
4. Increase the input voltage in the step of 1V up to 20V.
5. Plot the characteristics of input voltage and output voltage.

Antilog:



Procedure:

1. Set the input voltage to 100mV.
2. See the voltage across the Resistor. Note the negative sign.
3. Increase the input voltage in the step of 50mV up to 500mV.
4. Plot the characteristics of input voltage and output voltage.
5. Reverse the polarity of the diode and see the effect for positive input voltage.

Observation Table:

Input Voltage	Output Voltage

Result & Discussion: Graph is drawn and verified.

Experiment Number-4

Design of Voltage Comparator and Zero Crossing Detector

Aim: To design a Voltage comparator and Zero Crossing Detector.

Apparatus:

S.NO.	Name of the Equipment	Values	Quantity
1	Resistor	10KΩ	1
2	Resistor	1KΩ	2
3	Function Generator	1MHz	1
4	I.C. 741 OP-AMP		1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

Comparator:

A comparator circuit is one which compares a voltage signal at one input with a known reference signal at the other input. It works in open loop mode. There are basically two types of comparator namely inverting and non-inverting comparators. The output will be either $+V_{sat}$ or $-V_{sat}$ depending upon the amplitude of the signal at the input terminal. If the amplitude of the non-inverting terminal signal is greater than the inverting terminal signal then the output will be $+V_{sat}$ and vice-versa.

Zero Crossing Detector:

The zero crossing detector is a special case basic comparator circuit. If we set reference voltage zero then a comparator behaves like a zero crossing detector.

Design: Not required

PROCEDURE:

Comparator:

1. Connect the IC on the base and connect power supply on respective terminals.
2. Connect input signal through a resistor in series to inverting terminal and reference signal through a resistor to non inverting terminal.
3. Connect the load resistor to the output terminal and also the probe of CRO to the output terminal.

Observation Table: Not required

Zero Crossing Detector:

In comparator circuit set the reference voltage to ground and keep everything same.

Observation Table: Not Required

Result: The waveforms are verified and it satisfied the stated conditions.

VIVA QUESTIONS:

1. What is a comparator?
2. List the important characteristics of a comparator.
3. What is a zero crossing detector?
4. List some applications of a comparator.
5. What is the basic difference between a basic comparator and a Schmitt trigger?

Experiment Number-5

Design of Wien Bridge Oscillator using Operational Amplifier.

Aim: To design a Wien-bridge oscillator using operational amplifier having resonant frequency 965 Hz.

Apparatus:

S.NO.	Name of the Equipment	Values	Quantity
1	Resistor	10KΩ	1
2	Resistor	3.3 KΩ	1
3	Function Generator	1MHz	1
4	I.C. 741 OP-AMP		1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		
8	Potentiometer	50 kΩ	1

Theory/Design:

Suppose we have to design oscillator of resonant frequency 965 Hz.

We know that the resonant frequency f_0 is given by

$$f_0 = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

Let C = 0.05 μF therefore R will can be calculated as

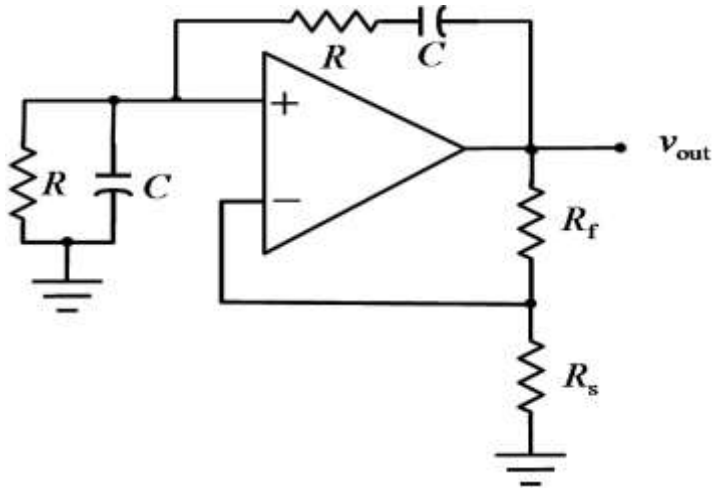
$$R = \frac{0.159}{(965)0.05*10^{-6}} = 3.3\ k\Omega$$

Let R_s = 10 kΩ

$R_f = 2R_s$

Therefore R_f = 20 kΩ

Circuit Diagram:



Procedure:

Connect the circuit as shown in figure and observe the output at pin number 6. Trace it on CRO screen.

Observation:

Trace the waveform and measure the frequency.

Result: Sinusoidal waveform was traced on pin 6 and verified with stated condition.

VIVA QUESTIONS:

1. Define an oscillator.
2. What are the two requirements for oscillation?
3. How are oscillators classifieds?
4. What is frequency stability? Explain its significance.

Experiment Number-6

Design of Monostable Multivibrator Circuit using 555 Timer:

AIM: To construct and study the operation of a monostable multivibrator using 555 IC timer.

APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	555 IC Timer		1
2	Resistor	10 KΩ	1
3	Capacitors	10nF, 0.1μF, 0.01μF	1
4	Function Generator	1MHz	1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

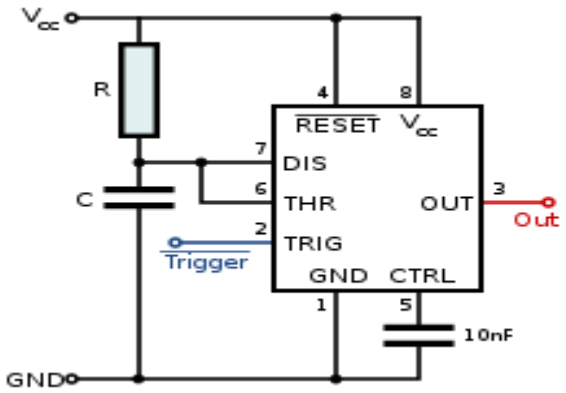
It has one stable and one quasi stable state. The circuit is useful for generating single output pulse of time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The diode gives a negative triggering pulse. When the output is +Vsat, a diode clamps the capacitor voltage to 0.7V then, a negative going triggering impulse magnitude Vi passing through RC and the negative triggering pulse is applied to the positive terminal. Let us assume that the circuit is instable state. The output V0i is at +Vsat. The diode D1 conducts and Vc the voltage across the capacitor 'C' gets clamped to 0.7V,the voltage at the positive input terminal through R1R2 potentiometer divider is +ßVsat. Now, if a negative trigger of magnitude Vi is applied to the positive terminal so that the effective signal is less than 0.7V.the output of the Op-Amp will switch from +Vsat to –Vsat. The diode will now get reverse biased and the capacitor starts charging exponentially to –Vsat. When the capacitor charge Vc becomes slightly more negative than –ßVsat, the output of the op-amp switches back to +Vsat. The capacitor 'C' now starts charging to +Vsat through R until Vc is 0.7V.

$V_0 = V_f + (V_i - V_f)\, e^{t/RC}$, ß = R2/(R1+R2)

If Vsat >> Vp and R1=R2 and ß = 0.5,

Then, T = 0.69RC

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in the circuit diagram.
2. Apply Negative triggering pulses at pin 2 of frequency 1 KHz as shown in Fig.
3. Observe the output waveform and capacitor voltage as shown in Figure and measure the pulse duration.
4. Theoretically calculate the pulse duration as $T_{high} = 1.1\ RC$
5. Compare it with experimental values.

Observation: Trace the time period of the output wave form and compare it with the given one.

Result & Discussion: The waveform is observed and verified with stated condition.

VIVA QUESTIONS:

1. Why is a monostable multivibrator called so?
   Ans: The monostable circuit has only one stable state (output low) hence the name monostable.
2. What is the purpose of monostable multivibrator?
   Ans: A monostable device, on the other hand, is only able to hold in one particular state indefinitely. Its other state can only be held momentarily when triggered by an external input.
3. Give one examples of multivibrator.
   Ans: The flip-flop is a free running multivibrator.
4. What is the principle of monostable multivibrator?
   Ans: All monostable multivibrators are timed devices. That is, their unstable output state will hold only for a certain minimum amount of time before returning to its stable state.
5. How does a monostable multivibrator work in terms of the astable multivibrator?
   Ans: Like the astable multivibrator, one transistor conducts and the others cut-off when the circuit is energized.

Experiment Number-7

Design of Astable Multivibrator Circuit using 555 Timer:

AIM: To construct and study the operation of a monostable multivibrator using 555 IC timer.

APPARATUS:

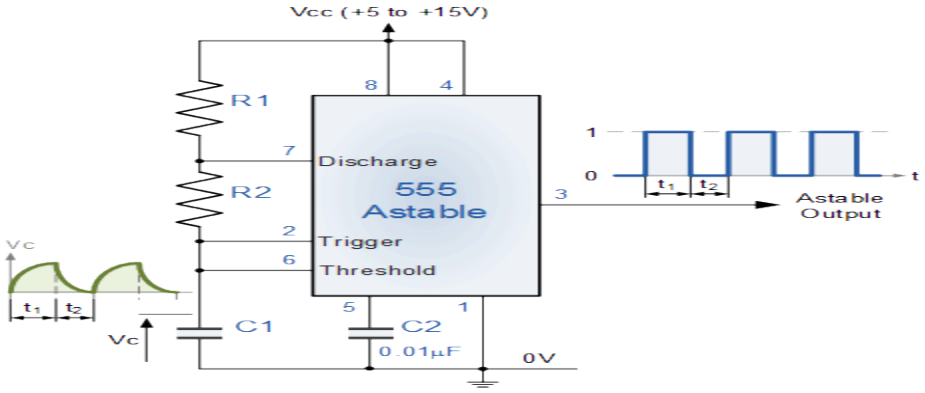
S.NO.	Name of the Equipment	Values	Quantity
1	555 IC Timer		1
2	Resistor	10 KΩ	1
3	Capacitors	10nF, 0.1µF, 0.01µF	1
4	Function Generator	1MHz	1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

In the 555 Oscillator above, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator. During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R_2 is connected to the discharge terminal, pin 7. Then the capacitor charges up to 2/3Vcc (the upper comparator limit) which is determined by the $0.693(R_1+R_2)C$ combination and discharges itself down to 1/3Vcc (the lower comparator limit) determined by the 0.693(R2.C) combination. This results in an output waveform whose voltage level is approximately equal to Vcc - 1.5V and whose output "ON" and "OFF" time periods are determined by the capacitor and resistors combinations. The individual times required completing one charge and discharge cycle of the output is therefore given as:

$t_1 = 0.693\ (R_1+R_2)C$, $t_2 = 0.693\ R_2C$, $T = t_1 + t_2$

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in the figure.
2. Use potentiometer in case output is not proper.

Observation: Trace the output waveform and calculate the frequency from the fundamental period of the wave.

Result & Discussion: The waveform was traced and compared with the designed theoretical one.

VIVA QUESTIONS:

1. What is an astable multivibrator called so?
   Ans: There is no stable state where the circuit can come to rest, so this circuit is known as an astable multivibrator.
2. How does a monostable multivibrator work in terms of the astable multivibrator?
   Ans: Like the astable multivibrator, one transistor conducts and the others cut-off when the circuit is energized.
3. What is the disadvantage of an astable multivibrator?
   Ans: When the astable m/v was first energized, it was impossible to predict which transistor would initially go to cut-off because of circuit symmetry.
4. What are the different types of multivibrator circuits?
   Ans: There are three types of m/v circuits: Astable, Monostable and Bistable.

Experiment Number – 8

Aim: To construct and study the voltage to current convertor.

Apparatus:

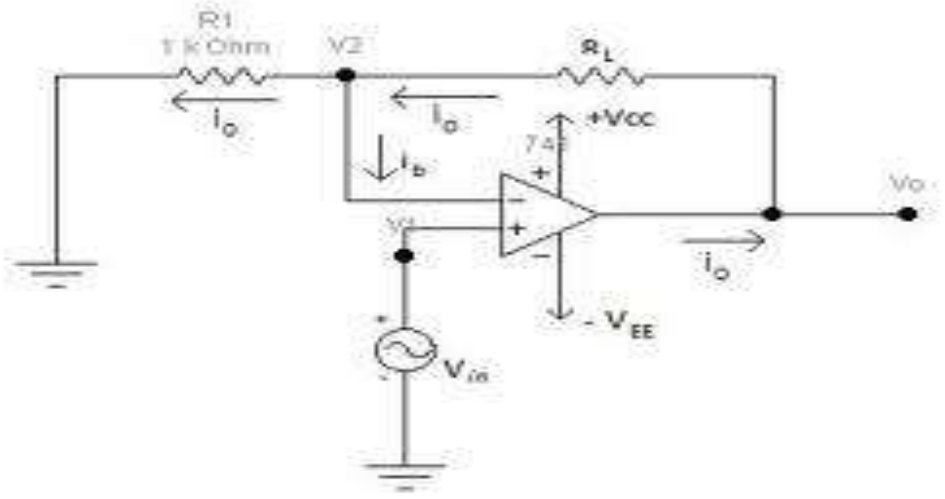
S.NO.	Name of the Equipment	Values	Quantity
1	Resistor	1KΩ, 10kΩ	1
2	Potentiometer	10 kΩ	1
3	Function Generator	1MHz	1
4	IC 741 OP-AMP		1
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

Theory: In the circuit shown in figure in which load R_L is floating. Since voltage at node 'a' is v_i, therefore,

$$i_L = \frac{v_i}{R1}$$

That is the input voltage v_i is converted into an output current of $\frac{v_i}{R_1}$. It may be seen that the same current flows through the signal source and load, therefore signal source should be capable of providing this load current.

Circuit Diagram:



Procedure:

1. Connect the circuit as shown in figure.
2. Connect a 10kΩ load resistor at the output pin number 6.
3. Connect an ammeter in series with R_L to measure the load current.

Observation Table:

Input Voltage (Volts)	Output Current (mA)

Result & Discussion: The graph between input voltage and output current is drawn and verified in linear range.

Experiment Number – 9

FUNCTION GENERATOR USING OP AMPS

AIM: To generate triangular and square wave forms and to determine the time period of the waveforms.

APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	Op-Amp IC 741		2
2	Resistor	10 KΩ,150kΩ,1.5kΩ,1MΩ,8.2kΩ	1
3	Capacitors	10nF, 0.1μF, 0.01μF	1
4	Zener diodes	6.2V	2
5	CRO	20 MHz	1
6	Bread Board		1
7	Connecting Wires and Probes		

THEORY:

The function generator consists of a comparator U1 and an integrator A2.The comparator U2 compares the voltage at point P continuously with the inverting input i.e., at zero volts. When voltage at P goes slightly below or above zero volts, the output of U1 is at the negative or positive saturation level, respectively. To illustrate the circuit operation let us set the output of U1 at positive saturation +Vsat (approximately +Vcc). This +Vsat is an input to the integrator U2. The output of U2, therefore will be a negative going ramp. Thus, one end of the voltage divider R2-R3 is the positive saturation voltage +Vast of U1 and the other is the negative going ramp of U2. When the negative going ramp attains a certain value –Vramp, point p is slightly below zero valts; hence the output of U1 will switch from positive saturation to negative saturation –Vsat (approximately –Vcc). This means that the output of U2 will now stop going negatively and will begin to go positively. The output of U2 will continue to increase until it reaches +Vramp. At this time the point P is slightly above zero volts. The sequence then repeats. The frequencies of the square are a function of the d.c supply voltage. Desired amplitude can be obtained by using approximate zeners at the output of U1.

THEORETICAL VALUES: Time period, $T= 4R_5C (R_3+R_4)/ (R_1+R_2) = 0.492$ msec.

Positive peak ramp = $VzR_5/ (R_1+R_2) = 0.05$ volts.

PRACTICAL VALUES:

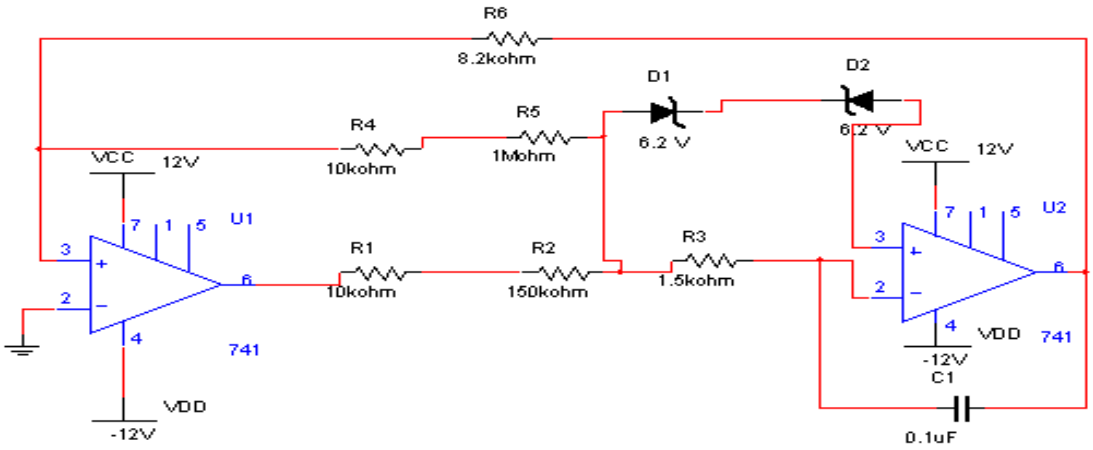
Time periods of triangular wave=

Time periods of square wave=

Positive peak ramp=

Voltage of square wave=

CIRCUIT DIAGRAM:



PROCEDURE:

1. The circuit is connected as shown in the figure.

2. The output of the comparator U1 is connected to the CRO through chennal1, to generate a square wave.

3. The output of the comparator U2 is connected to the CRO through chennal2, to generate a triangular wave.

4. The time periods of the square wave and triangular waves are noted and they are found to be equal.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.

2. Maintain proper Vcc levels.

RESULT: The theoretical and practical values of time periods are found to be equal.

VIVA QUESTIONS:

1. Define function generator?
2. Write some applications of function generator?
3. What is the function of function generator?
4. Draw the block diagram of function generator?

Experiment Number –10

4 BIT DAC USING OP AMP

AIM: To construct and study digital to analog converter circuit.

APPARATUS:

S.NO.	Name of the Equipment	Values	Quantity
1	Op-Amp IC 741		2
2	Resistors	1 KΩ,2kΩ,4kΩ,8kΩ,10kΩ	5 each
3	Multimeter		
4	CRO	20 MHz	1
5	IC Bread Board Trainer		1
6	Connecting Wires and Probes		

Theory: A digital to analog converter is used when a binary output from a digital system must be converted to equivalent analog voltage or current. A DAC converter uses an op-amp and binary weighted resistors or R-2r ladder resistors.
In binary weighted resistors method are used. This can be avoided by using R-2R ladder type DAC where only 2 values of resistors are required .The binary inputs are simulated by switches B0-B3 and output is proportional to the binary inputs. Binary inputs can be high (+5V) or low (0V).

PROCEDURE:

1. Connections are made as per circuit diagram.

2. Pin2 is connected to resistor 1MΩand ground.

3. +Vcc are available at Pin7 and –Vcc is applied at Pin4.

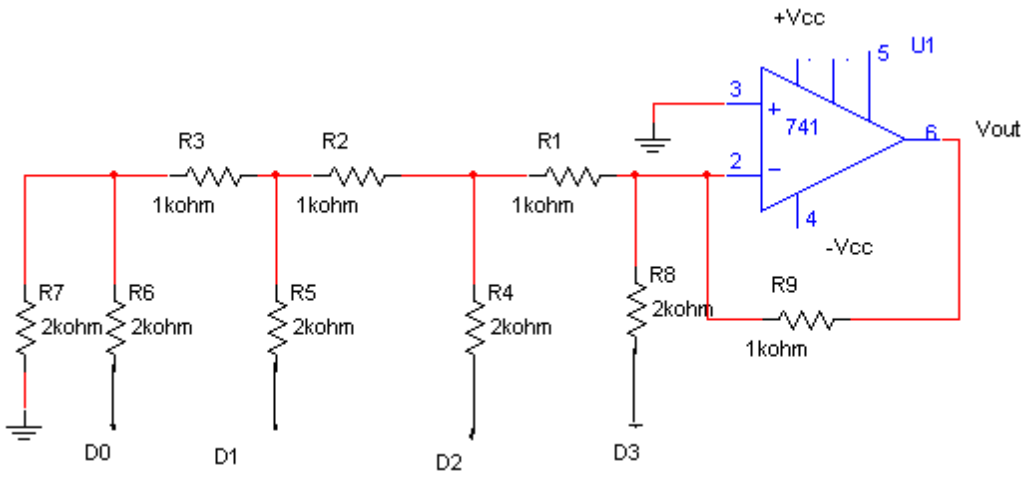
4. Output is taken between pin6 and ground

5. Voltage at each bit (vr) is found at bits b0, b1, b2, b3.

6. Pin3 of op amp is connected to resistor 1kΩ and is given to b3 (MSB).

7. A resistor of 2kΩ is connected between pin2 and pin 6 of op amp.

CIRCUIT DIAGRAM:



Observation:

D_3	D_2	D_1	D_0	Analog Output	
				Theoretical	Practical

RESULT: Thus digital to analog converter is constructed and studied.

VIVA QUESTIONS:

1. What is meant by resolution of DAC?

2. What is meant by linearity of DAC?

3. What is meant by accuracy of DAC?

4. What is meant by DAC?

5. What is disadvantage of weighted resistor DAC?

6. What is the value of resistor required in weighted resistor DAC if LSB resistor value is 12KΩ for 4 bit DAC?

7. What are the applications of DAC?