DRONACHARYA
Group of Institutions

CIRCUIT SIMULATION

LABORATORY MANUAL

B.Tech. 3rd Semester

Subject Code: BEE-351

Session: 2023-24, Odd Semester

DRONACHARYA GROUP OF INSTITUTIONS
DEPARTMENT OF EEE
#27 KNOWLEDGE PARK 3

GREATER NOIDA

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List of Experiments mapped with COs

Si No.	Name of the Experiment	Course Outcome
1	Verification of principle of Superposition with AC sources using Multisim/ PSPICE.	CO 1
2	Verification of Thevenin and Maximum Power Transfer theorems in AC Circuits using Multisim/ PSPICE.	CO 1
3	Verification of Norton theorems in AC Circuits using Multisim/ PSPICE.	CO 2
4	Verification of Tellegen's theorem for two networks of the same topology using Multisim/ PSPICE.	CO 2
5	Determination of Z and h-parameters (DC only) for a network and computation of Y and ABCD Parameters using Multisim/ PSPICE.	CO 3
6	Determination of driving point and transfer functions of a two port ladder network and verify with theoretical values using Multisim/ PSPICE.	CO 2
7	Determination of transient response of current in RL and RC circuits with step voltage input.	CO 4
8	Determination of transient response of current in RLC circuit with step voltage input for under damped, critically damped and over damped cases.	CO 2
9	Determination of image impedance and characteristic impedance of T and Π networks, using O.C. and S.C. tests.	CO 3
10	Verification of parameter properties in inter-connected two port networks: series, parallel and cascade using Multisim/ PSPICE.	CO 2

LAB EXPERIMENTS

LAB EXPERIMENT 1

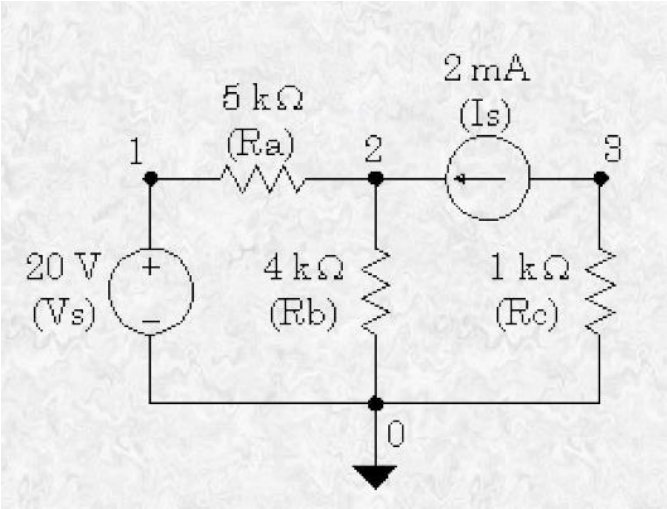
AIM: To Simulate the DC Circuit for determining the all node voltages using PSPICE.

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram **with I**ntegrated **C**ircuit **E**mphasis.

PROGRAM:

```
Vs    1    0    DC    20.0V
Ra    1    2    5.0k
Rb    2    0    4.0k
Rc    3    0    1.0k
Is    3    2    DC    2.0mA
.END
```

CIRCUIT DIAGRAM:



OUTPUT :

```
NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE
VOLTAGE( 1) 20.0000 ( 2) 13.3330 ( 3) -2.0000 <==
Results
```

```
VOLTAGE SOURCE

CURRENTSNAME CURRENT
Vs -1.333E-03 <== Current entering node 1 of Vs

TOTAL POWER DISSIPATION 2.67E-02

WATTSJOB CONCLUDED
TOTAL JOB TIME .26
```

RESULT:

LAB EXPERIMENT 2

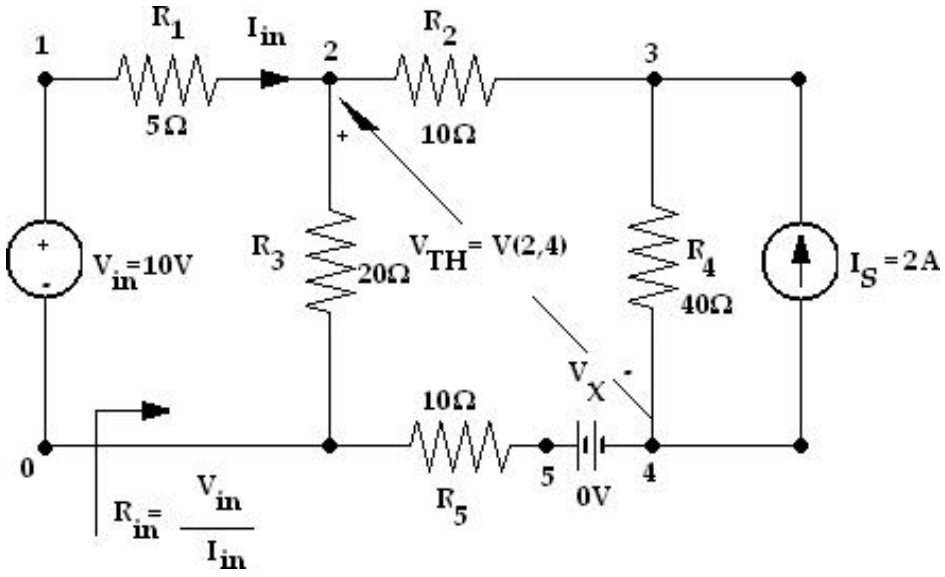
AIM: To Simulate the DC Circuit for determining the Thevenin's equivalent and Norton's equivalent using PSPICE.

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram **with I**ntegrated **C**ircuit **E**mphasis.

DATA REQUIRED FOR DRAWING CIRCUIT DIAGRAM:

A DC Circuit is as shown in the figure. It Consists of Voltage Source whose Value is **10V;** the Current source has the Value of **2A.** It has the resistance values as **5Ω**, **10Ω, 20Ω, 40Ω, and 10Ω** respectively. Use PSPICE to plot and calculate the Thevenin's Equivalent Circuit across the nodes **2** and **4.**Obtain the transfer function between the two nodes **2** and **4.**

CIRCUIT DIAGRAM:



PROGRAM:

Thevenins theorem :

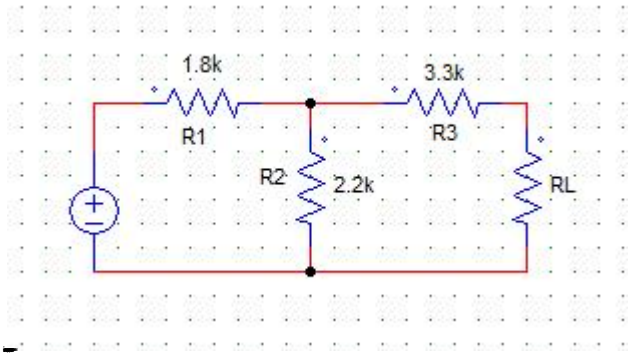
*

```
VIN 1 0 DC 10V
IS 4 3 2A
VX 4 5 DC 0V
R1 1 2 5
R2 2 3 10
R3 2 0 20
R4 3 4 40
R5 5 0 10
.TF V(2,4) VIN
.END
```

Norton's theorem :

CIRCUIT

DIAGRAM:



OUTPUT:

RESULT:

LAB EXPERIMENT 3

AIM: To Simulate the DC network with sub circuit using PSPICE.

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram **with I**ntegrated **C**ircuit **E**mphasis.

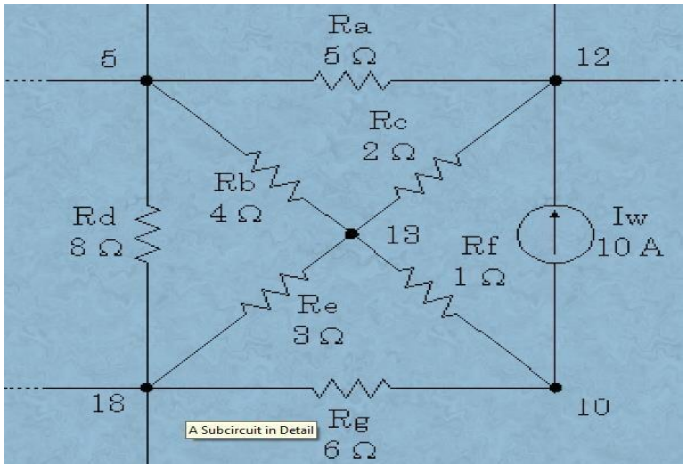
THEORY :

Coding a Subcircuit

Each subcircuit used in a study must have a unique name. This is true of any othercircuit element. Also, there must be a list of at least two nodes that can be connected to elements external to the subcircuit. A subcircuit can have many external node connections, if needed. Later, we will find that parameters can be passed to a subcircuit in order to allow unique behavior and responses from an instance of a subcircuit.

The initial line of a subcircuit section must begin with ".SUBCKT," followed by the name and then the external node list. After that, optional features (not to be discussed yet) can be added. The best method of understanding the use of a subcircuit is by example. Below, we find a cluster of components that can be combined into a subcircuit.

Sub circuit:



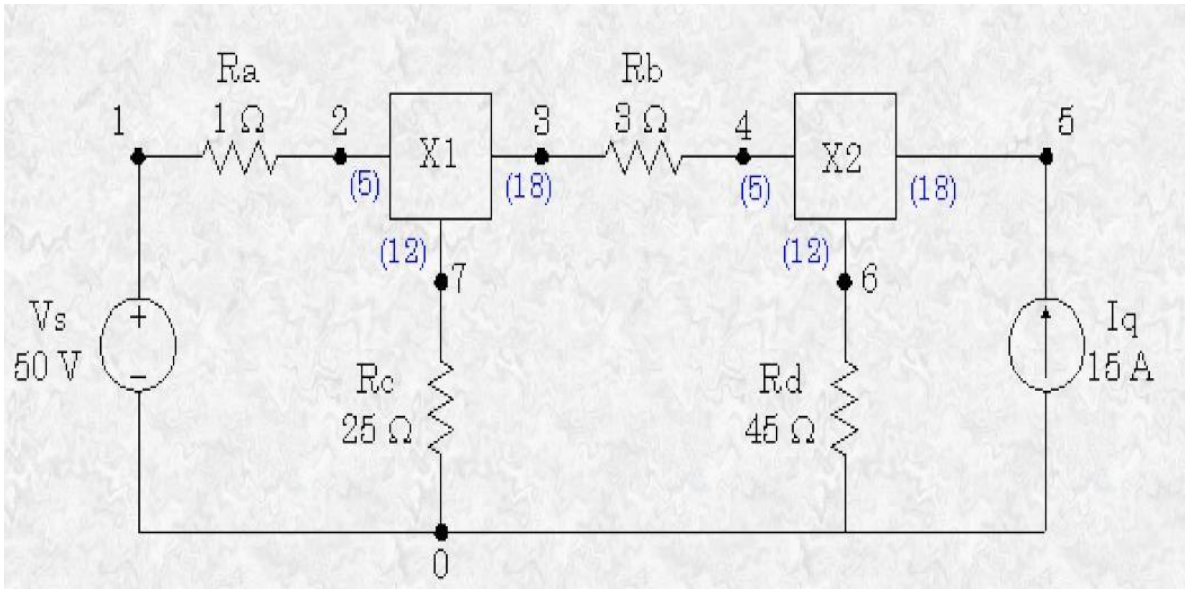
Note that nodes 5, 12 and 18 have external connections. Therefore, they must beincluded in the node list in the subcircuit definition. Nodes 10 and 13 do not have external connections and need not be (indeed *should* not be) included in this node list. They are internal nodes and will be used to help define the subcircuit.

Now, we can code the above subcircuit as follows. Note that the code could beembedded into the rest of the code for the main circuit or could be placed in aseparate *include* file.

Program for sub circuit:

```
.SUBCKT Example_1    5    12    18
Iw     10     12     DC     10A
Ra      5     12     2.0
Rb      5     13     5.0
Rc     12     13     2.0
Rd      5     18     8.0
Re     13     18     3.0
Rf     10     13     1.0
Rg     10     18     6.0
.ENDS
```

Main circuit diagram:



Main program:

```
6.0.ENDS
Vs 1 0 DC 50V
Ra 1 2 1.0
Rb 3 4 3.0
```

```
Rc 7 0 25.0
Rd 6 0 45.0
X1 2 7 3
X2 4 6 5
.END
```

OUTPUT:

RESULT:

LAB EXPERIMENT 4

AIM: To find out the transient response and parametric analysis by simulationof RLC circuits Using Pulse, and Step response

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

a) Simulation of STEP RESPONSE Using PSPICE:

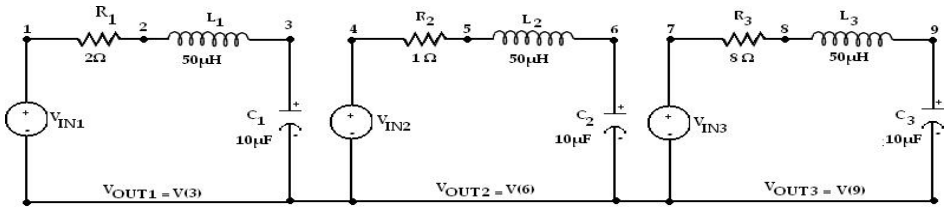
SYNTAX USED:

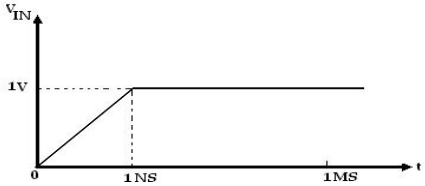
S.NO	TYPE OF SOURCE	REPRESENTATION OF SOURCE	DECLARATION FORMAT
1.	STEP RESPONSE	PWL	STEP (Time at a Point) (Voltage at a Point)
2.	TRANSIENT ANALYSIS	.TRAN	.TRAN TStep Tstop [TStart TMax] [UIC]
3.	PROBE STATEMENT	.PROBE	It is a wave form analyzer
4.	PLOT STATEMENT	.PLOT	.PLOT (Output Variables) {(Lower limit Value), (Upper Limit Value)}

DATA REQUIRED FOR DRAWING THE CIRCUIT DIAGRAM:

For example, Three RLC circuits with R=**2Ω**, **1 Ω**, and **8 Ω** respectively, with L having the values of **50µH** each, with C having the values of **10µF** each. The inputs are identical **Step Response.** The Step having the Time at points as **1nsec** and **1msec** respectively and Voltage at a point as **1V** respectively. Use PSPICE to plot and calculate the transient response from **0** to **400µseconds** with an increment of **1µsecond**. Plot the voltages across the capacitors

CIRCUIT DIAGRAM:





PROGRAM:

```
*
VIN1 1 0 PWL(0 0 1NS 1V 1MS 1V)
VIN2 4 0 PWL(0 0 1NS 1V 1MS 1V)
VIN3 7 0 PWL(0 0 1NS 1V 1MS 1V)
R1 1 2 2
R2 4 5 1
R3 7 8 8
L1 2 3 50UH
L2 5 6 50UH
L3 8 9 50UH
C1 3 0 10UF
C2 6 0 10UF
C3 9 0 10UF
.TRAN 1US 400US
.PLOT TRAN V(3) V(6) V(9)
.PROBE
.END
```

OUTPUT:

RESULT: Analysis of Series RLC Circuit with STEP Response has beensuccessfully completed.

b) Simulation of PULSE RESPONSE Using PSPICE:

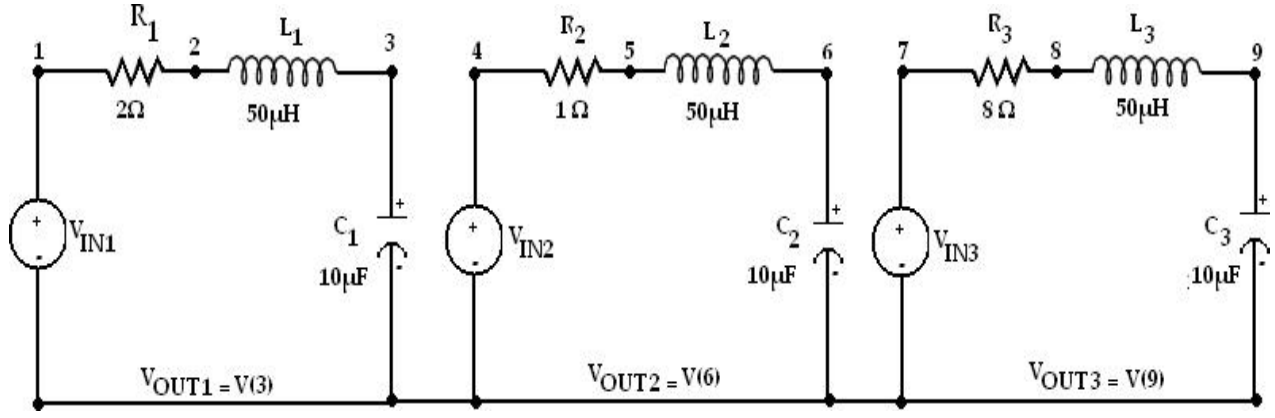
SYNTAX USED:

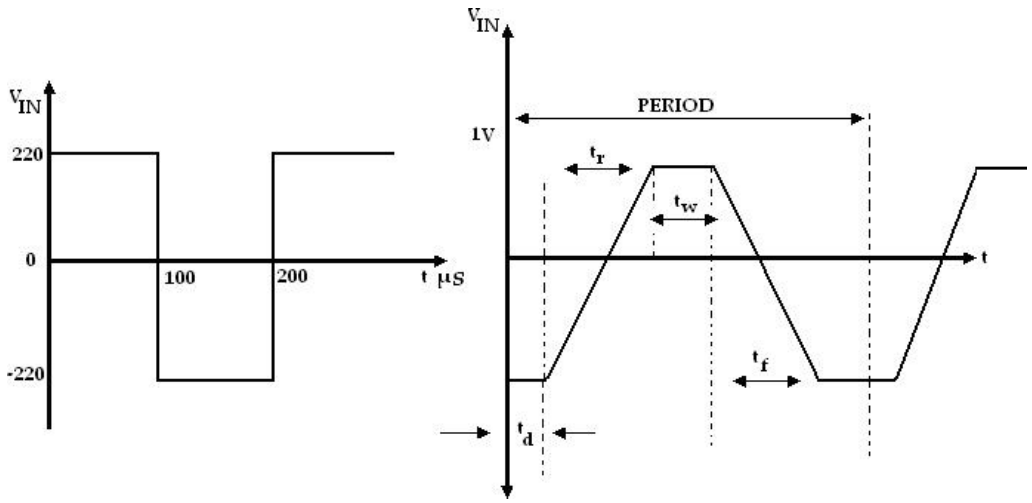
S.NO	TYPE OF SOURCE	REPRESENTATION OF SOURCE	DECLARATION FORMAT
1.	PULSE RESPONSE	PULSE	PULSE (Initial Value) (Pulsed Value) (Delay Time)(Rise Time)(Fall Time) (Pulse Width) (period)
2.	TRANSIENT ANALYSIS	.TRAN	.TRAN TStep Tstop [TStart TMax] [UIC]
3.	PROBE STATEMENT	.PROBE	It is a wave form analyzer
4.	PLOT STATEMENT	.PLOT	.PLOT (Output Variables) {(Lower limit Value), (Upper Limit Value)}

DATA REQUIRED FOR DRAWING THE CIRCUIT DIAGRAM:

For example, Three RLC circuits with R=**2Ω**, **1 Ω**, and **8 Ω** respectively, with L having the values of **50μH** each, with C having the values of **10μF** each. The input is **Pulse Response.** The Pulse having the Initial voltage as **-10V**, Pulsed Voltage as **10V,** Delay Time as **1nsec,** Rise Time as **1nsec,**Fall Time as **1nsec,** Pulse Width as **100μSeconds**, and Period as **200μseconds**.Use PSPICE to plot and calculate the transient response from **0** to **400μseconds** with an increment of **1μsecond**. Plot the voltages across the capacitors.

CIRCUIT DIAGRAM:





PROGRAM:

*

VIN1 1 0 PULSE(-220 220 0 1NS 1NS 100US 200US)
VIN2 4 0 PULSE(-220 220 0 1NS 1NS 100US 200US)
VIN3 7 0 PULSE(-220 220 0 1NS 1NS 100US 200US)
R1 1 2 2
R2 4 5 1
R3 7 8 8
L1 2 3 50UH
L2 5 6 50UH
L3 8 9 50UH
C1 3 0 10UF
C2 6 0 10UF
C3 9 0 10UF
.TRAN 1US 400US
.PLOT TRAN V(3) V(6) V(9)
.PROBE
.END

OUTPUT:

RESULT: Analysis of Series RLC Circuit with PULSE Response has beensuccessfully completed.

LAB EXPERIMENT 5

AIM: To find out the transient response and parametric analysis by simulationof RLC circuits Using Sinusoidal Responses.

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

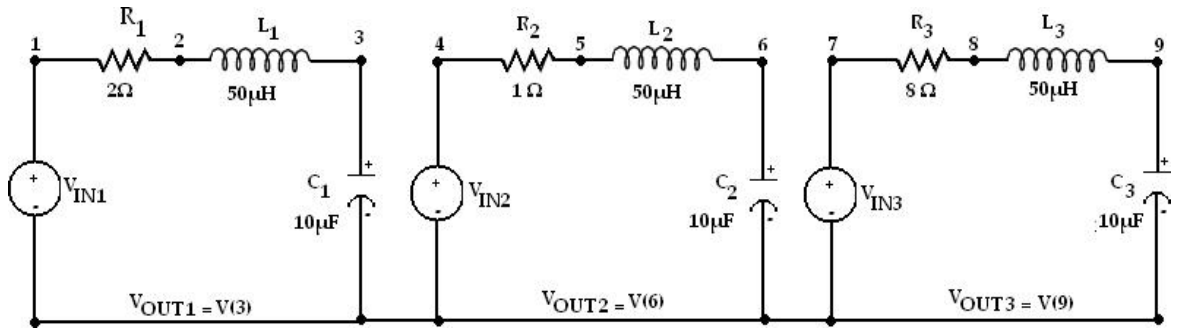
SYNTAX USED:

S.NO	TYPE OF SOURCE	REPRESENTATION OF SOURCE	DECLARATION FORMAT
1.	SINUSOIDAL RESPONSE	SIN	SIN (Offset Value) (Peak Value) (Frequency)(Delay Time) (DampingFactor) (Phase Delay)
2.	TRANSIENT ANALYSIS	.TRAN	.TRAN TStep Tstop [TStart TMax]
3.	PROBE STATEMENT	.PROBE	It is a wave form analyzer
4.	PLOT STATEMENT	.PLOT	.PLOT (Output Variables) {(Lower limit Value), (Upper Limit Value)}

DATA REQUIRED FOR DRAWING THE CIRCUIT DIAGRAM:

For example, Three RLC circuits with R=**2Ω**, **1 Ω**, and **8 Ω** respectively, with L having the values of **50µH** each, with C having the values of **10µF** each. The inputs are identical **Sinusoidal Response.** The Sinusoidal response having the offset voltage as **0V,** RMS voltage as **120V** and the frequency as **50Hz**. Use PSPICE to plot and calculate the transient response from **0** to **60mseconds** with an increment of **1µsecond**. Plot the voltages across the capacitors.

CIRCUIT DIAGRAM:



PROGRAM:

```
*
VIN1 1 0 SIN(0 169.7V 50)
VIN2 4 0 SIN(0 169.7V 50)
VIN3 7 0 SIN(0 169.7V 50)
R1 1 2 2
R2 4 5 1
R3 7 8 8
L1 2 3 50UH
L2 5 6 50UH
L3 8 9 50UH
C1 3 0 10UF
C2 6 0 10UF
C3 9 0 10UF
.TRAN 1US 400US
.PLOT TRAN V(3) V(6) V(9)
.PROBE
.END
```

OUTPUT:

RESULT: Analysis of Series RLC Circuit with Sinusoidal Response has been successfully completed.

LAB EXPERIMENT 6

AIM: To analyse three phase currents and the neutral current by the analysis of three phase circuit representing the Generator, Transmission line and loads using PSPICE.

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram **with I**ntegrated **C**ircuit **E**mphasis.

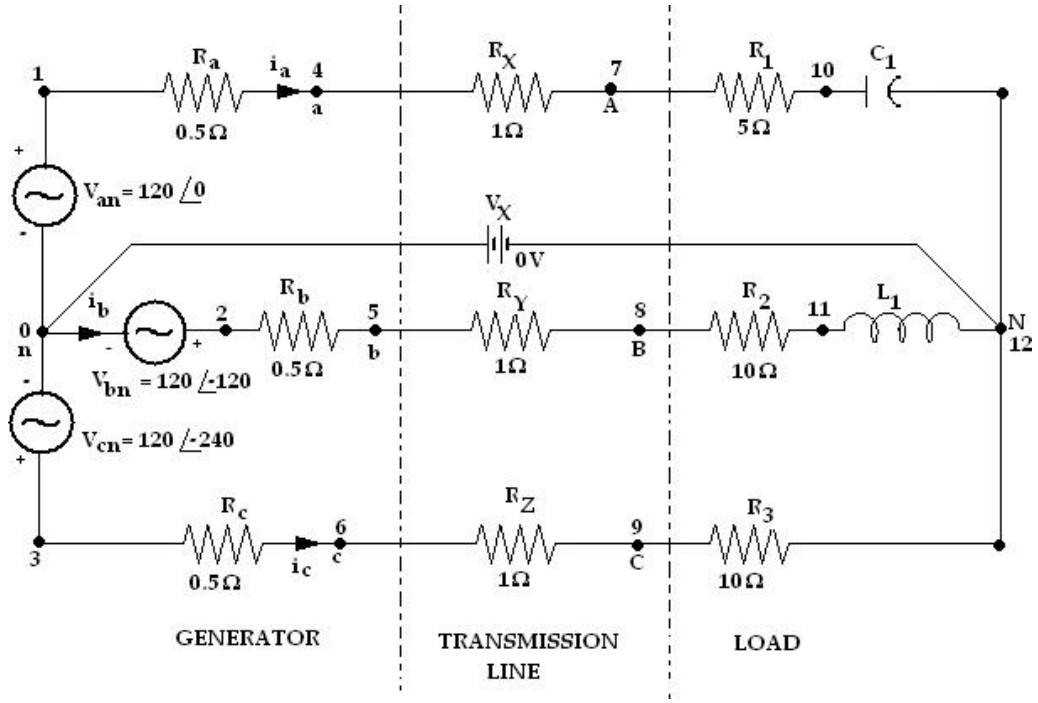
SYNTAX USED:

S.NO	TYPE OF SOURCE	REPRESENTATION OF SOURCE	DECLARATION FORMAT
1.	SINUSOIDAL RESPONSE	SIN	SIN (Offset Voltage) (Peak Voltage) (Frequency)(Delay Time) (Damping Factor) (Phase Delay)
2.	TRANSIENT ANALYSIS	.TRAN	.TRAN TStep Tstop
3.	PROBE STATEMENT	.PROBE	It is a wave form analyzer
4.	PLOT STATEMENT	.PLOT	.PLOT (Output Variables) {(Lower limit Value), (Upper Limit Value)}

DATA REQUIRED FOR DRAWING CIRCUIT DIAGRAM:

For example, the circuit consists of Generators, transmission lines and loads. It is fed with a three phase balanced supply. Arrange the generators in STAR connection and connect the Transmission lines and loads to it. The generator is having a resistance of **0.5Ω** and the transmission line is having a resistance of **1 Ω** and consists of loads having $\mathbf{R_1=10\Omega}$, $\mathbf{R_2=10\Omega}$, and $\mathbf{R_3=10\Omega}$ respectively, $\mathbf{L_1=120mH}$ and $\mathbf{C_1=120\mu F}$. The Sinusoidal having the offset voltage as **0V,** RMS voltage as **120V,** the frequency as **60Hz,** the Delay Time and the Damping Factor are given as **0** and the Phase angle as $\mathbf{120^0}$. Use PSPICE to plot the instantaneous currents. Plot the transient response from **0** to **50mseconds** with an increment of **5μsecond**.

CIRCUIT DIAGRAM:



PROGRAM:

*

VIN1 1 0 SIN(0 169.7V 50)
VIN2 2 0 SIN(0 169.7V 50 0 0 120)
VIN3 3 0 SIN(0 169.7V 50 0 0 240)
RA 1 4 0.5
RB 2 5 0.5
RC 3 6 0.5
RX 4 7 1
RY 5 8 1
RZ 6 9 1
R1 7 10 5
R2 8 11 10
R3 9 12 10
VX 12 0 DC 0V
.TRAN 5US 50MS
.PLOT TRAN I(RA) I(RB) I(RC)
.PROBE
.END

OUTPUT:

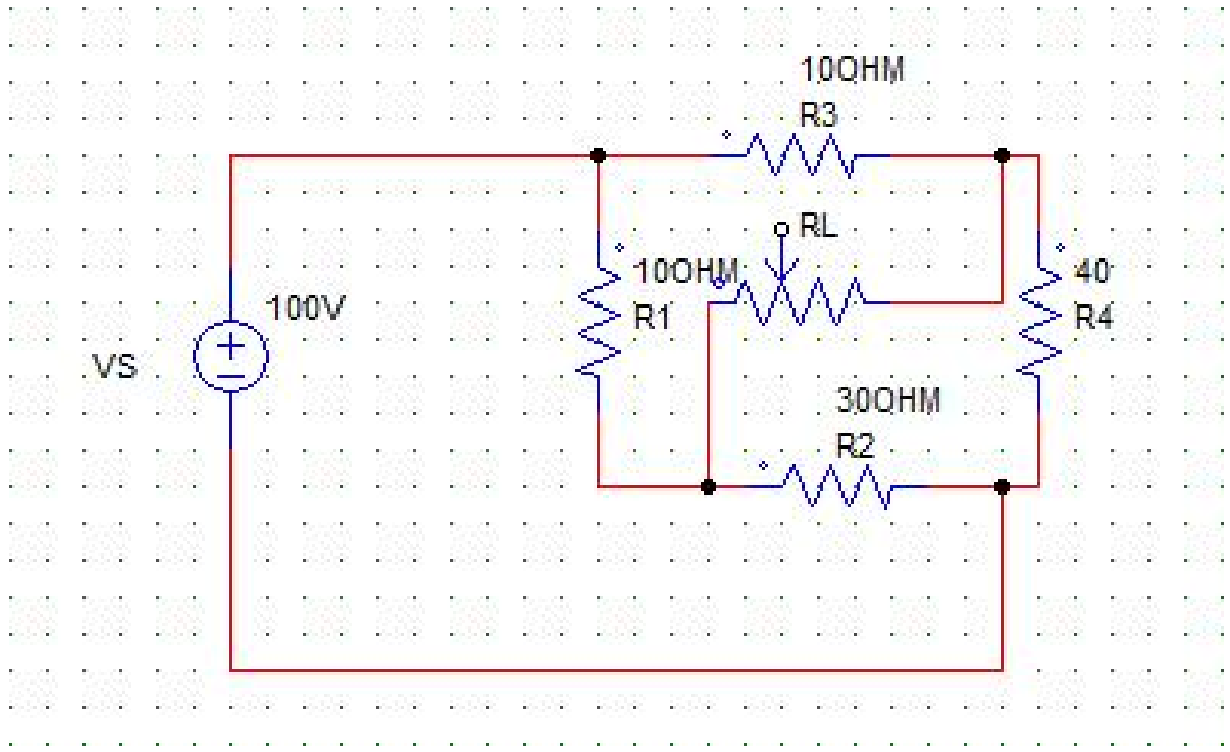
RESULT:

LAB EXPERIMENT 7

AIM: To find out the unknown resistance and maximum power for dc circuits

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

CIRCUIT DIAGRAM:



Program:

```
*
VS 1 0 DC 100
R1 1 2 10
R2 2 0 30
R3 1 3 20
R4 3 0 40
RL 2 3 RLOAD 1
.MODEL RLOAD RES(R=25)
```

.
DC RES RLOAD(R) 0.001 40 0.01
.TF V(2,3) VS
.PROBE
.END

OUTPUT:

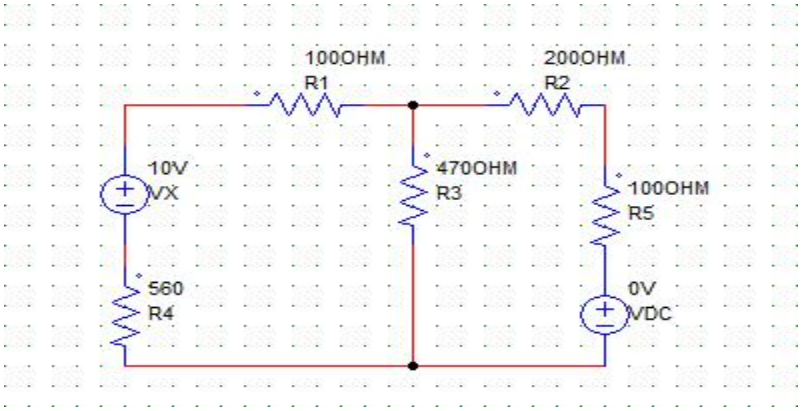
RESULT:

LAB EXPERIMENT 8

AIM: To verify the reciprocity theorem for dc circuits

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

Circuit diagtam:



FOR MAIN CIRCUIT:

FOR CIRCUIT 1:

```
*
VX 1 2 DC 0V

R1 1 3 100
R2 3 4 200
R3 3 0 470
R4 2 0 560
R5 4 5 100
VDC  5 0 DC 10V
.OP
.END
```

OUTPUT:'

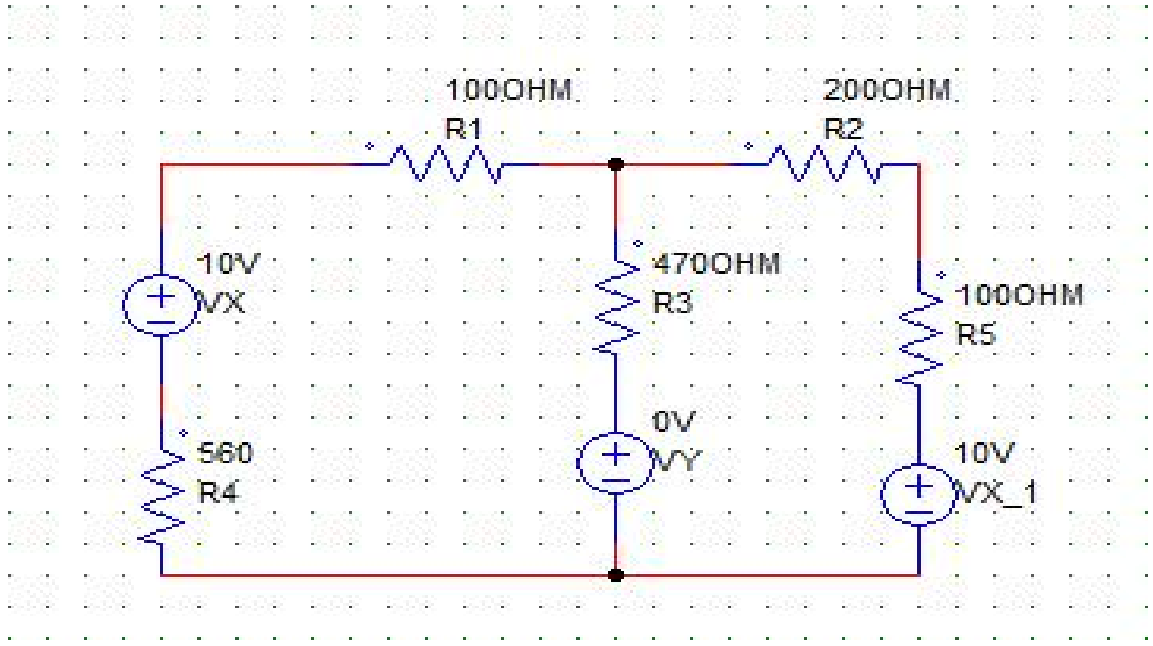
RESULT:

LAB EXPERIMENT 9

AIM: To verify the superposition theorem for dc circuits

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

CIRCUIT DIAGRAM:



Program:
FOR MAIN CIRCUIT :

```
*
VDC 1 2 DC 10V
R1 1 3 100
R2 3 4 200
R3 3 6 470
R4 2 0 560
R5 4 5 100
VX 5 0 DC 10V
VY 6 0 DC 0V
.OP
.END
```

FOR CIRCUIT 1:

```
*
VDC 1 2 DC 10V
R1 1 3 100
R2 3 4 200
R3 3 6 470
R4 2 0 560
R5 4 0 100
VY 6 0 DC 0V
.OP
.END
```

FOR CIRCUIT 2:

```
*
VDC 1 2 DC 0V
R1 1 3 100
R2 3 4 200
R3 3 6 470
R4 2 0 560
R5 4 5 100
VX 5 0 DC 10V
VY 6 0 DC 0V
.OP
.END
```

OUTPUT:

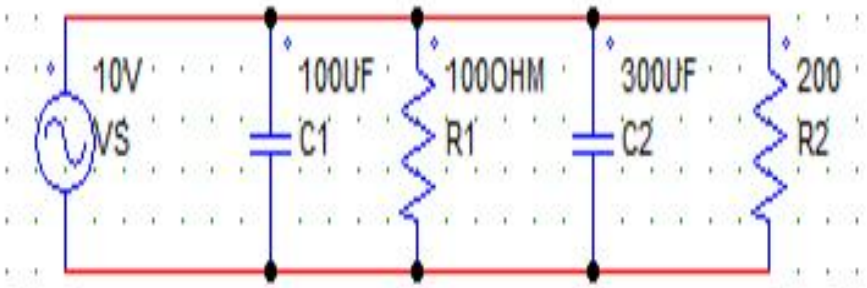
RESULT:

LAB EXPERIMENT_10

AIM: To calculate the responce for the ac circuits.

SOFTWARE REQUIRED: **PSPICE – P**ersonal Computer **S**imulated **P**rogram with **I**ntegrated **C**ircuit **E**mphasis.

CIRCUIT DIAGRAM:



Program:

```
*
VS 1 0 AC 10V
C1 1 0 100U
R1 1 0 100
C2 1 0 300U
R2 1 0 200
.AC LIN 1 50 100
.PRINT AC IM(VS) IP(VS) IM(C1) IP(C1)
.END
```

OUTPUT:

RESULT:

LAB EXPERIMENT 11

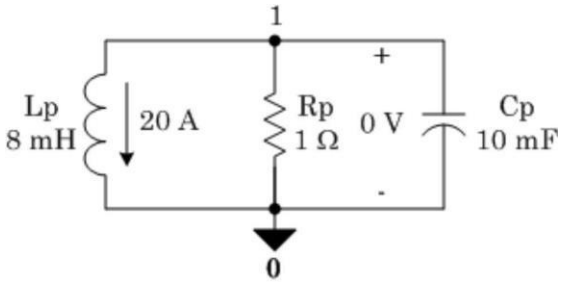
OBJECTIVE: To obtain transient response of a parallel R-L-C circuit for step current input.

SOFTWARE REQUIRED:

PSPICE VERSION 8

CIRCUIT & PROGRAM:

One of the most interesting aspects of circuit analysis is the study of natural and step responses of circuits and the responses of circuits to time-varying sources. To perform these analyses we introduce another group of "dot" commands



Use of the .TRAN command

This is the command that passes the user's parameters for performing the transient analysis on a circuit to the PSpice program. There are four time parameters and an instruction to use the initial conditions rather than calculated bias point values for starting conditions. First, we show a sample .TRAN statement and then we will describe its parameters.

```
* prt_stp t_max prt_dly max_stp
.TRAN 20us 20ms 8ms 10us UIC
```

In the above statement, the "20us" value labeled "prt_stp" *(print step)* is the frequency with which data is saved. In this case, the system variables are stored each 20μs of simulation time. The actual time steps used by PSpice may be different from this. The second parameter, "20ms," labeled as "t_max" *(final time)* is the value of time at which the simulation will be ended. Since PSpice starts at t = 0, there will be a total of 20ms time span of simulation for the circuit. The third parameter, "8ms," labeled as "prt_dly" *(print delay)* is the print delay time. In some cases, we do not want to store the data for the entire time span of the simulation. In our sample statement shown above, we ignore the data from the first 8ms of simulation and then store the data for the last 12ms. Most of the time, this parameter is set to zero or not used. The fourth parameter, "10us," labeled as "max_stp" *(max step)* is the maximum time step size PSpice is allowed to take during the simulation. Since PSpice automatically adjusts its time step size during the simulation, it may increase the step size to a value greater than desirable for displaying the data.

When the variables are changing rapidly, PSpice short- ens the step size, and when the variables change more slowly, it increases the step size. Use of this parameter is optional. The last parameter in our list is "UIC." It is an acronym for "UseInitial Conditions."

Unless you include this parameter, PSpice will ignore the initial condi- tions you set for your inductors and capacitors and will use its own calculated bias point in- formation instead. Note that the use of the letter "s" after the numbers in the .TRAN statement is optional. PSpice assumes these values are seconds and actually ignores the "s." However, it is recommended that you use units until you are extremely familiar with all of these commands and definitions.
Now, we will examine some more .TRAN examples.

```
.TRAN 10ns 500us
```

In the above example, PSpice will save data at each 10ns interval of the simulation starting at t = 0 until the final time of 500μs. I.e., there is no print delay and the user has given full control of the calculation step size to PSpice. In addition, PSpice will calculate its own initial conditions for any inductors and capacitors, ignoring any initial conditions set by the user.

```
.TRAN 50m 2.5 0 10m UIC
```

In the above statement, PSpice collects the data at each 50ms time interval starting from zero up to 2.5s. A zero was required as as a placeholder for the print delay parameter since the maximum step size of 10ms was specified. PSpice will use the designated initial conditions of capacitor voltage and inductor current. Notice that the units were left off the numbers in this statement. Only the prefixes which size the values are needed.

Use of the .PROBE command
In addition to specifying the time parameters for a transient solution of a circuit problem, we need to specify how the data is to be saved. In most cases, this simply means that we include a line in the *.CIR file consisting of ".PROBE." This instructs PSpice to create a data file and store the data it calculates. If we create a circuit listing named "CIRCUIT1.CIR" containing a ".TRAN" statement and a ".PROBE" statement, PSpice will create a file named "CIRCUIT1.DAT" holding the data as well as the usual "CIRCUIT1.OUT" file with basic information about the circuit. By default, the data file created by PSpice is a binary data file; i.e., you can't read it with a text editor. This is the most efficient way of saving the data. However, there is an optional parameter (/CSDF) for the .PROBE statement that causes PSpice to save the data in a Common Simulation Data Format which is a text format that allows you to look at the raw data with a text editor.

However, it will take up more space and PROBE doesn't load it for graphing. You will need to make a second run without the /CSDF parameter if you want to plot the data.
Also by default, .PROBE causes *all* the circuit variables to be saved, including all the variables inside each instance of each subcircuit. In some cases, this can amount to a lot of data. If you simulate a large complex circuit with many parts and need to save data at short time intervals over a very long time span, you can easily create gigabyte-size "DAT" files. To avoid this, you can specify the values you want to save. If the

".PROBE" command is issued without any parameters, everything is saved. If you specify the quantities you want saved, *only* those quantities will be saved. We will now examine some .PROBE statements.

```
.PROBE
```

All the above statement does is the enable PSpice to save everything in a binary DAT file.

```
.PROBE/CSDF
```

The above statement enables PSpice to save everything in a CSDF file that can be opened (and edited) with a text editor. You can

```
.PROBE V(5,23) I(Rx) I(L4)
```

The above statement tells PSpice to save only the voltage drop between nodes 5 and 23, the current through resistor, Rx, and the current through inductor, L4, all in binary format. No other data will be saved.

RESULTS & DISCUSSION:

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Please spare some time to provide your valuable feedback.