DRONACHARYA
GROUP OF INSTITUTIONS

LABORATORY MANUAL

DIGITAL COMMUNICATION LAB

SUBJECT CODE:BEC-651

B.TECH. (ECE) SEMESTER-VI

AcademicSession:2024-25,EvenSemester

StudentName:	
Roll. No.:	
Branch/Section:	

Dronacharya Group of Institutions

PlotNo.27,Knowledge Park-3,GreaterNoida,UttarPradesh201308

Affiliated to

Dr.APJ Abdul Kalam Technical University

Lucknow, Uttar Pradesh226031

Table of Contents

Vision of the Institute

"Instilling core human values and facilitating competence to address global challenges by providing Quality Technical Education.

Mission of the Institute

- M1 - Enhancing technical expertise through innovative research and education, fostering creativity and excellence in problem-solving.
- M2 - Cultivating a culture of ethical innovation and user-focused design, ensuring technological progress enhances the well-being of society.
- M3 - Equipping individuals with the technical skills and ethical values to lead and innovate responsibly in an ever-evolving digital landscape.

.

Program Educational Objectives (PEOs)

- To apply the scientific, mathematical and engineering fundamentals to provide solutions to the problems in Electronics and Communication Engineering and related fields.
- To exhibit creativity and innovation with ethical and professional behavior while addressing societal needs by engaging technocrats in independent learning.
- To empower technocrats by nurturing ethical values, creativity, and innovation, enabling them to pursue entrepreneurship or higher studies and establish their own startups, thereby impacting their lives positively.

Program Outcomes (POs)

The successful graduate will develop ability to:

- **PO1. Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
- **PO2. Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- **PO3. Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
- **PO4. Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- **PO5. Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
- **PO6. The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- **PO7. Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
- **PO8. Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
- **PO9. Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
- **PO10. Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write

effective reports and design documentation, make effective presentations, and give and receive clear instructions.

- **PO11. Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- **PO12. Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcome (PSOs)

- To apply fundamental knowledge of core Electronics and Communication Engineering subjects in the analysis, design, and development of various types of electronic systems.
- To adapt to modern software and hardware tools in Electronics and Communication Engineering for the design and analysis of complex electronic systems and their real-life applications.
- To prepare students to adjust in evolving work environments, effective interpersonal abilities, adherence to professional ethics and awareness of societal needs.

University Syllabus

1. **Part A**

1. To study Eye diagram patterns of various digital pulses.
2. To study the Inter symbol interference.
3. To study generation of Unipolar RZ & NRZ Line Coding.
4. To study generation of Polar RZ & NRZ Line Coding.
5. To study generation of Bipolar RZ & NRZ Line Coding.
6. Implementation and analysis of BASK modulation and demodulation
7. Implementation and analysis of BFSK modulation and demodulation
8. Implementation and analysis of BPSK modulation and demodulation. (Through Virtual Lab)
9. Implementation and analysis of QPSK modulation and demodulation. (Through Virtual Lab)
10. To simulate M-ary Phase shift keying technique using MATLAB.
11. To study generation and detection of DPSK using MATLAB.
12. Implementation and analysis of Delta modulation and demodulation.
13. Implementation and analysis of DSSS Modulation, Demodulation & BER measurement.
14. Implementation and analysis of FHSS Modulation, Demodulation & BER measurement.
15. To study encoding and decoding of Linear Block Codes
16. To study the working of Convolution encoder.

Part B

1. To study simple dipole 2 antenna and to calculate beam-width, front /back ratio, and gain of the antenna. 10.
2. Tostudyfoldeddipoleantennaandtocalculatebeam-width,front/backratio,andgainofthe antenna.
3. To study 2 phase array end-fire antenna and to calculate beam-width, front / back ratio, and gain of the antenna.
4. To study broad side array antenna and to calculate beam-width, front/ back ratio, and gain of the antenna.

Course Outcomes

CO-1	To formulate basic concepts of pulse shaping in digital communication.
CO-2	To identify different line coding techniques and demonstrate the concepts.
CO-3	Todesignequipmentsrelatedtodigitalmodulationanddemodulationschemes.
CO-4	To analyze the performance of various digital communication systems and evaluate the key parameters.
CO-5	To conceptualize error detection & correction using different coding Schemes in digital communication.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	2	1	2		2	2			1
CO2	2	2	1			1						
CO3	2	3	3	2	2	3		2	2			2
CO4	2	2						2	2			2
CO5	3	2	3	3	2	3		1	1			2
Course Correlation mapping	**2.4**	**2.4**	**1.8**	**1.4**	**1**	**1.8**		**1.4**	**1.4**			**1.4**

Correlation Levels: High-3, Medium-2, Low-1

CO-PSO Mapping

	PSO1	PSO2	PSO3
CO1	3	3	2
CO2	3	3	2
CO3	2	3	2
CO4	2	2	1
CO5	2	2	1
	2.4	**2.6**	**1.6**

Course Overview

In this lab students will be able to learn about the concept of Eye diagram patterns of various digital pulses, the inter symbol interference, generation of Unipolar RZ & NRZ Line Coding, generation of Polar RZ & NRZ Line Coding, generation of Bipolar RZ & NRZ Line Coding, Implementation and analysis of BASK modulation and demodulation, Implementation and analysis of BFSK modulation and demodulation, Implementation and analysis of BPSK modulation and demodulation, Implementation and analysis of QPSK modulation and demodulation, M-ary Phase shift keying technique using MATLAB, generation and detection of DPSK using MATLAB, Implementation and analysis of Delta modulation and demodulation, Implementation and analysis of DSSS Modulation, Demodulation & BER measurement, Implementation and analysis of FHSS Modulation, Demodulation & BER measurement, study of encoding and decoding of Linear Block Codes as well as working of Convolution encoder and antennas.

List of Experiments mapped with COs

S.No	Aim of the Experiments	COs
1.	BASK Modulation and Demodulation	**CO1**
2.	BFSK Modulation and Demodulation	**CO1**
3.	Phase shift keying	**CO3**
4.	Differential Phase Shift Keying (Modulation and Demodulation)	**CO2**
5.	M-ary Phase shift keying	**CO3**
6.	Binary phase shift keying	**CO2**
7.	QPSK modulation & demodulation	**CO4**
8.	Delta modulation	**CO1**
9.	Linear block code-encoder & decoder	**CO1**
10.	Eye Diagrams, Noise and Bit Error Rate	**CO1**

DOs and DON'Ts

DOs

1. Proper dress has to be maintained while entering in the Lab. (Boys Tuck in and shoes and girls should be neatly dressed)
2. Students should carry observation notes and record completed in all aspects.
3. Circuit diagram, tabular Colum and model graph should be in the observation before entering the lab.
4. Circuit and its theoretical result should be there in the observation before coming to the next lab.
5. Students must maintain silence while doing experiments.
6. Student should follow the lab procedure and get the components from the lab instructor.
7. After completing the experiment need to switch off the power supply, return the components to lab instructor safely and arrange the chairs properly.
8. The Practical Result should be noted down into their observations and result must be shown to the Lecturer In-Charge for verification.
9. Students must ensure that all switches are in the OFF position; main switch is shut down properly.

DON'Ts

1. Don't come late to the Lab.
2. Don't leave the Lab without making proper shut down of power supply and return safely to lab instructor.
3. Don't disrupt others while doing experiments.
4. Don't leave the Lab without verification by Lab instructor.
5. Don't leave the lab without the permission of the Lecturer In-Charge.

General Safety Precautions

Precautions (In case of Injury or Electric Shock)

1. To break the victim with live electric source, use an insulator such as firewood or plastic to break the contact. Do not touch the victim with bare hands to avoid the risk of electrifying yourself.
2. Unplug the risk of faulty equipment. If the main circuit breaker is accessible, turn the circuit off.
3. If the victim is unconscious, start resuscitation immediately, use your hands to press the chest in and out to continue breathing function. Use mouth-to-mouth resuscitation if necessary.

Precautions (In case of Fire)

1. Turn the equipment off. If the power switch is not immediately accessible, take plug off.
2. If fire continues, try to curb the fire if possible, by using the fire extinguisher or by covering it with a heavy cloth if possible isolate the burning equipment from the other surrounding equipment.
3. Sound the fire alarm by activating the nearest alarm switch located in the hall way.

Guidelines to Students for Report Preparation

All students are required to maintain a record of the experiments conducted by them. Guidelines for its preparation are as follows:-

1) All files must contain a title page followed by an index page. ***The files will not be signed by the faculty without an entry in the index page.***

2) Student's Name, Roll number and date of conduction of experiment must be written on all pages.

3) For each experiment, the record must contain the following

(i) Aim/ Objective of the experiment

(ii) Pre-experiment work (as given by the faculty)

(iii) Lab assignment questions and their solutions

(iv) Test Cases (if applicable to the course)

(v) Results/ output

Note:

1. Students must bring their lab record along with them whenever they come for the lab.

2. Students must ensure that their lab record is regularly evaluated.

1. BASK Modulation and Demodulation

Aim: Implementation and analysis of BASK modulation and demodulation.

Software required: MATLAB

THEORY

MATLAB (matrix laboratory) is a multi-paradigm numerical computing environment and fourth-generation programming language. A proprietary programming language developed by Math Works, MATLAB allows matrix manipulations, plotting of functions and data, implementation of algorithms, creation user interfaces, and interfacing with programs written in other languages, including C, C++, Java, Fortran and Python.

MATLABPROGRAM:

```
clc
clearall;
closeall;
%GENERATECARRIERSIGNAL
Tb=1;
fc=10;
t=0:Tb/100:1
c=sqrt(2/Tb*sin(2*pi*fc*t);
%generatemessagesignal
N=8;
m=Tand(1.N);
tl=0:2=Tb
for  i=1:N
t=tl:01:12
ifmi)>0.5
m(i)=l:
m_s=ones(1,length();
else
m(i)=0;
```

```
m_s=zeros(1,length(t);
end
message(4:)=m_s;
bproductofcarrierandmessage
ask sigli,:)=c.*m_s;
tla1+(Tbt.01):
t2a2+(Tb+.0);
oplotthemessageandASKsignal
subplot(5,1,2);axis(|0 N -2 2):
plot(t,message(i.:),r);
title('messagesignal);
xlabelt->);
ylabel'm(t)):grid on
hold on
subploa(5,1,4);
plot(t,ask_sig(i.:)):
title('ASK signal);
xlabel't->);
ylabel('s(t)):gridon
hold on
end
holdoff
DPlatthecarriersignalandinputbinarydata
subplot(5,1,3);
plot(t.c):
title(carriersignal);
xlabel't-.>);
ylabe'e(t );:grid on
subplo(5,l,):stem(m);
title(binarydatabits'):
xlabel('n-);
ylabel('b(n)):grid on
```

```
6ASKDemodulation
tl=0:12=Tb
fori=1:N
=t1:Tb/1O0:12]
ocorrelator
x=sum(c.*ask_sig(i.:)):
%decisiondevice
if x>0demodi)=l;
else
demod(i)=0;
end
tlalHTb+.01);
t22(Tb+.01);
end
```

Result:

2. BFSK Modulation and Demodulation

Aim: Implementation and analysis of BFSK modulation and demodulation.

Software required: MATLAB

THEORY:

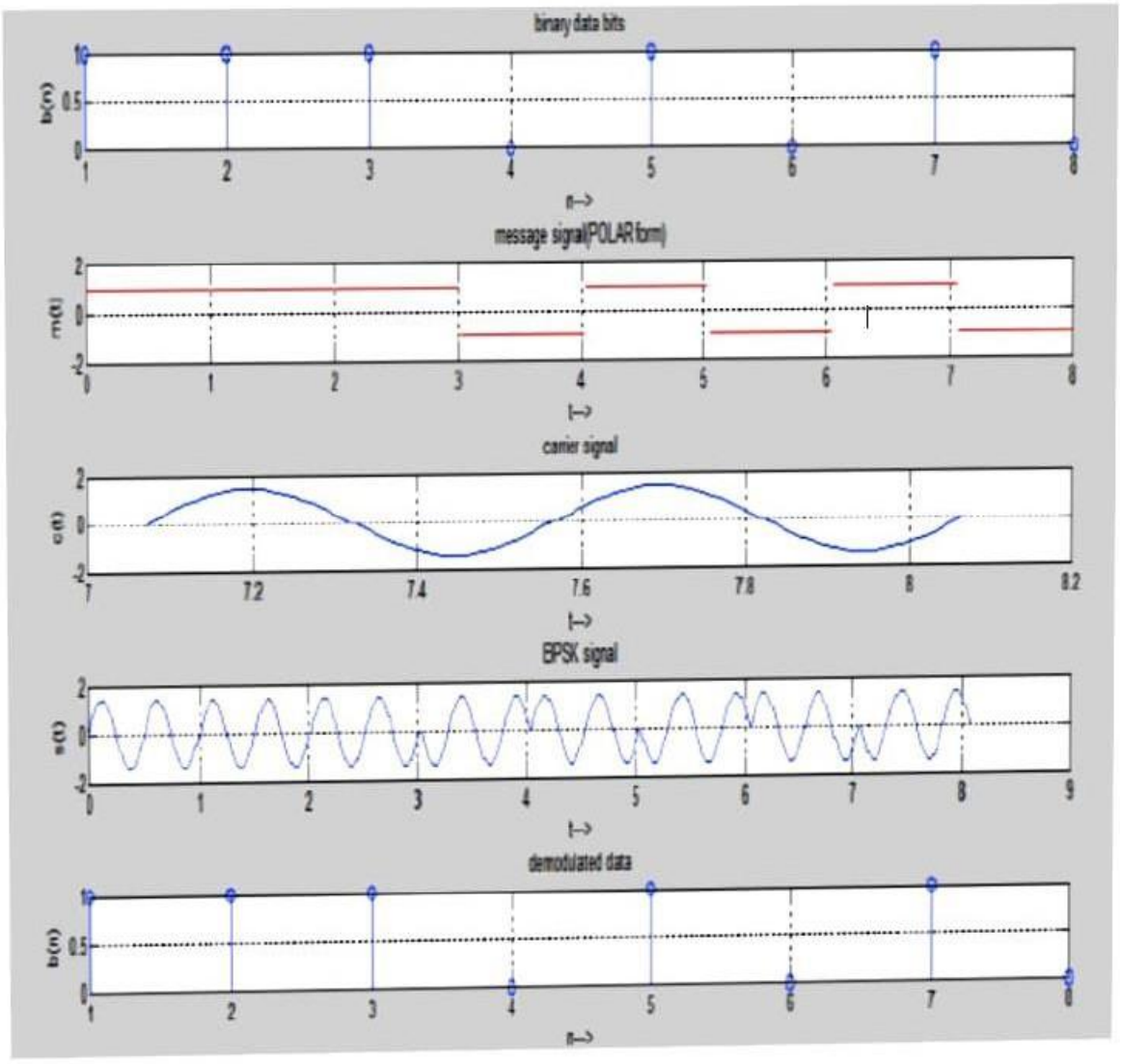
Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier signal. The technology is used for communication systems such as amateur radio, caller ID and emergency broadcasts. The
Simplest FSK is binary FSK (BFSK). BFSK uses a pair of discrete frequencies to transmit binary (Os and 1s) information. With this scheme, the "I" is called the mark frequency and the "o" is called the space frequency. This is simulated in MATLAB.

MATLABPROGRAM:

```
%PSK modulation
clc:
clear al
closeall;
GENERATECARRIERSIGNAL Tb=1;
t=0:Tb/10:Tb;
fc=2:
c=sqrt(2/Tb)*sin(2*pi*fc*t);
o generate message signal
N=8:
m=rand(1,N);
tl=0:t2=Tbfor
i=1:N
t=[t:.01:2]
ifm(i)>0.5
mi=l;
m_s=ones(1,length(t);
else
i)=0;
m_s=-1*ones(1,length(t);
end
message(i.:)=m_s;
%productofcarrierandmessagesignal
bpsk_sigi.:)=c.*m_s;
KPlotthemessageandBPSKmodulatedsignal
subplot(5,1.2
axis([ON-2 2):
```

```
plot(t.message(i.:),
r)xtitle('messagesignal(POLARfor
m): xlabel('t:
ylabel(m(t))%
gridon;holdon;
subplot(5,1,4);
plott.bpsk_sig(i.:)%
title(BPSK signal);
xlabel('t->');
ylabel('s(t))xgrid
on;holdon;
tlal+1.01;12=t2+1.01;
end
holdoff
bplottheinputbinarydataandcarriersignal subplot(5,
1., );stem(m);
title('binarydatabits')
xlabel('n-->);
ylabel('b(n)'):
grid on;
subplot(5,I.3);
plot(t.c):
title('carriersignal');
xlabel(t;
ylabel(c()):grid on
%PSKDemodulation
tl=0:t2=Tb
orri=1:N
=[tl:01:2
hcorelator
x=sum(c.tbpsk_sig(i.:)):
decision device
if x>0
demodi)=l;
else
demod(i)=0;
end
tl=tl+1.01;
t2=t2+1.0l;
end
oplotthedemodulateddatabits
subplot(5,1.5);stem(demod):
title('demodulated data)
xlabel('n-->);
ylabel('b(n)):grid on
```

OUTPUTWAVEFORM:



Result:

3. Phase Shift Keying

AIM

To study the operation of PHASE SHIFT KEYING modulation and demodulation .

INTRODUCTION

Digital communications became important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites. Phase Shift Keying (PSK) is a relatively new system, in which the carrier may be phase shifted by +180 degrees for a mark, and by −180 degrees for a space. PSK has a number of similarities to FSK in many aspects, as in FSK , frequency of the carrier is shifted according to the modulating square wave.

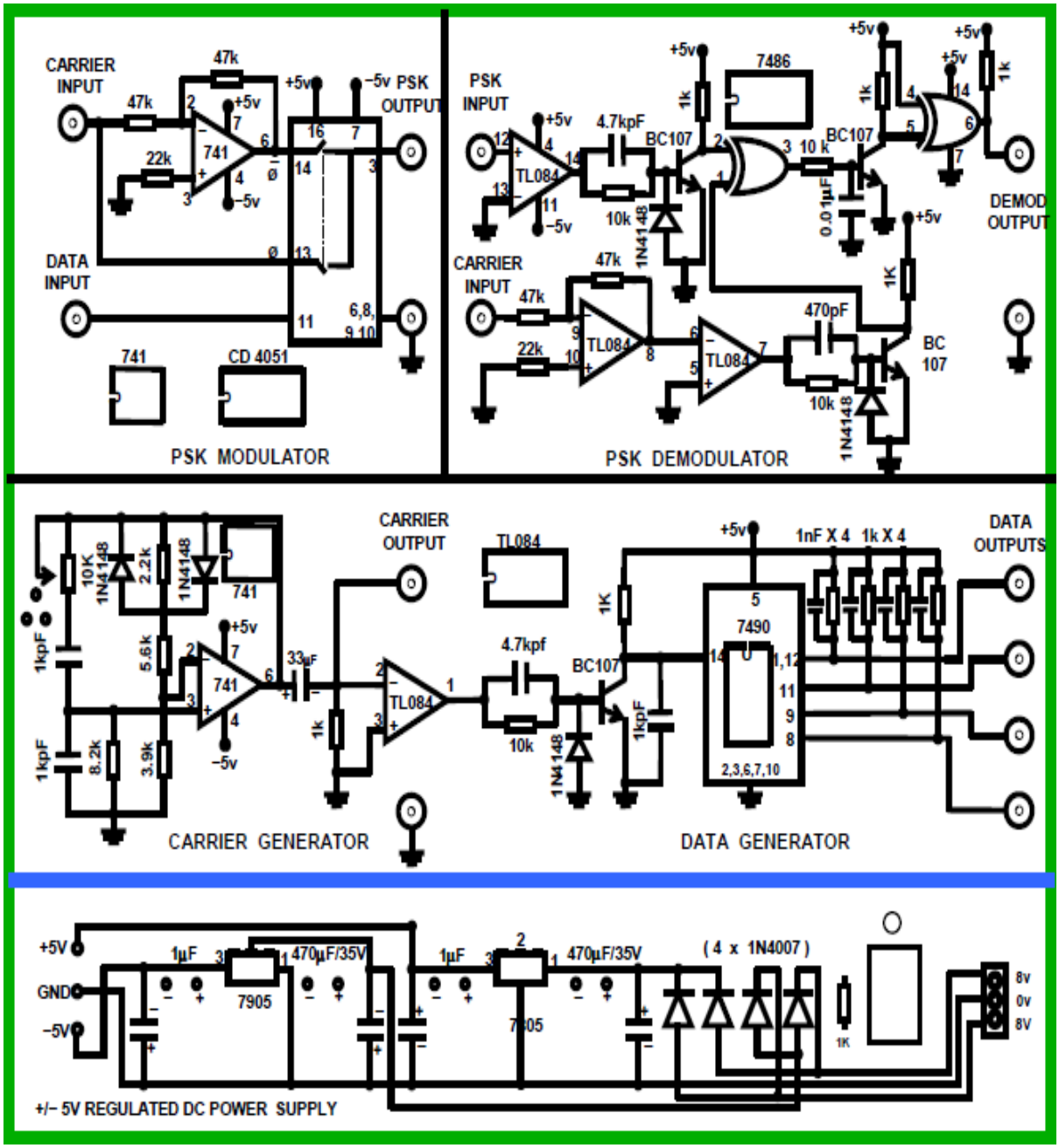
THEORY

Fig−1 shows the circuit diagram of the Phase Shift Key modulation and demodulation. In this carrier Generator is generated by a wein bridge oscillator around 28 KHz. At ± 5Vp−p sine wave using 741 IC.The sine wave is converted into square wave using TL084 in comparator mode. The transistor BC107 converts the square wave signal to TTL level. This is used as a basic bit clock or 180^0 for a mark and 0^0 for space.This square wave is used as a clock input to a decade counter (IC7490) which generates the modulating data outputs. IC CD4051 is an Analog multiplexer to which carrier is applied with and without 180° phase shift to the two multiplex inputs of the IC. Modulating data input is applied to its control input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered the output. The 180° phase shift to the carrier signal created by an operational amplifier using 741 IC. During the demodulation, the PSK signal is converted into a + 5 volts square wave signal using a transistor and is applied to one input of an EX − OR gate. To the second input of the Logic gate, carrier signal is applied after conversion into a +5 volts signal. So the EX − OR gate output is equivalent to the modulating data signal.

Phase shift keying is a digital modulation scheme that conveys data by changing, or modulating, the phase of a reference signal (the carrier wave).

Any digital modulation scheme uses a finite number of distinct signals to represent digital data. PSK uses a finite number of phases, each assigned a unique pattern of binary bits.

Circuit Diagram:



Usually, each phase encodes an equal number of bits. Each pattern of bits forms the symbol that is represented by the particular phase. The demodulator, which is designed specifically for the symbol set used by the modulator determines the phase of the received signal and maps it back to the symbol its represents, thus recovering the original data. This requires the receiver o able to compare the phase of the received signal to a reference signal.

HARDWARE SPECIFICATIONS

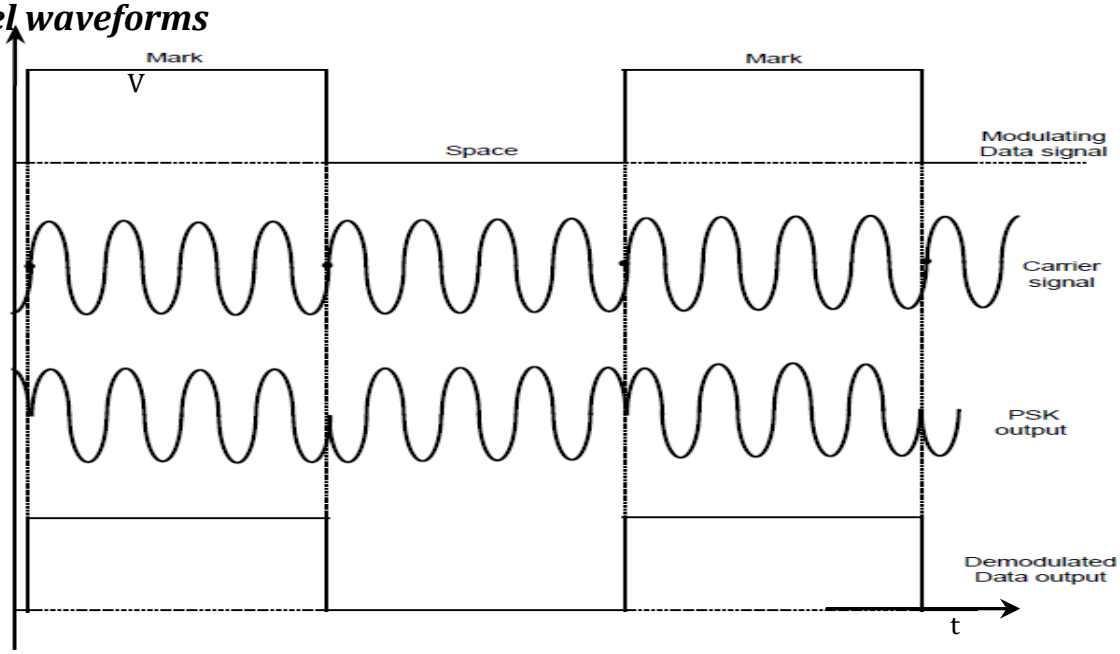
1) Panel lay out diagram with components mounted on PCB / panel.
2) Built in DC power supplies ± 5V/ 350mA.
3) Provided with 2mm sockets.
4) ICs provided on the board are 741, 7490, TL084, CD4051 & 7486.
5) Set of patch chords

   2mm Stackable patch chrods – 8 Nos.
6) user manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer. Switch 'ON' the power.
2. Apply the carrier signal to the input of the modulator.
3. Apply the modulating data signal to the modulator input and observe this signal on channel 1 of the CRO.
4. Observe the output of the PSK modulator on the channel 2 of the CRO.
5. Apply this PSK output to the demodulator input and also apply the carrier input.
6. Observe the demodulator output and compare it with the modulating data signal applied to the modulator input which is identical.

Model waveforms



PSK Signal Waveforms

PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT:

Thus the PSK modulation signal is generated for a given input data signal and it is demodulated.

4. Differential Phase Shift Keying Modulation and Demodulation

AIM

To study the various steps involved in generating the differential binary signal and differential phase shift keyed signal at the modulator end and recovering the binary signal from the received DPSK signal.

INTRODUCTION

Digital communications became important with the expansion of the use of computers and data processing, and have continued to develop into a major industry providing the interconnection of computer peripherals and transmission of data between distant sites.

Phase shift keying (PSK) is a relatively a new system, in which the carrier is phase shifted by + 90 degrees for a mark, and by -90 degrees for a space.

PSK has a number of similarities to FSK in many aspects, as in FSK, frequency of the carrier is shifted according to the modulating data level.

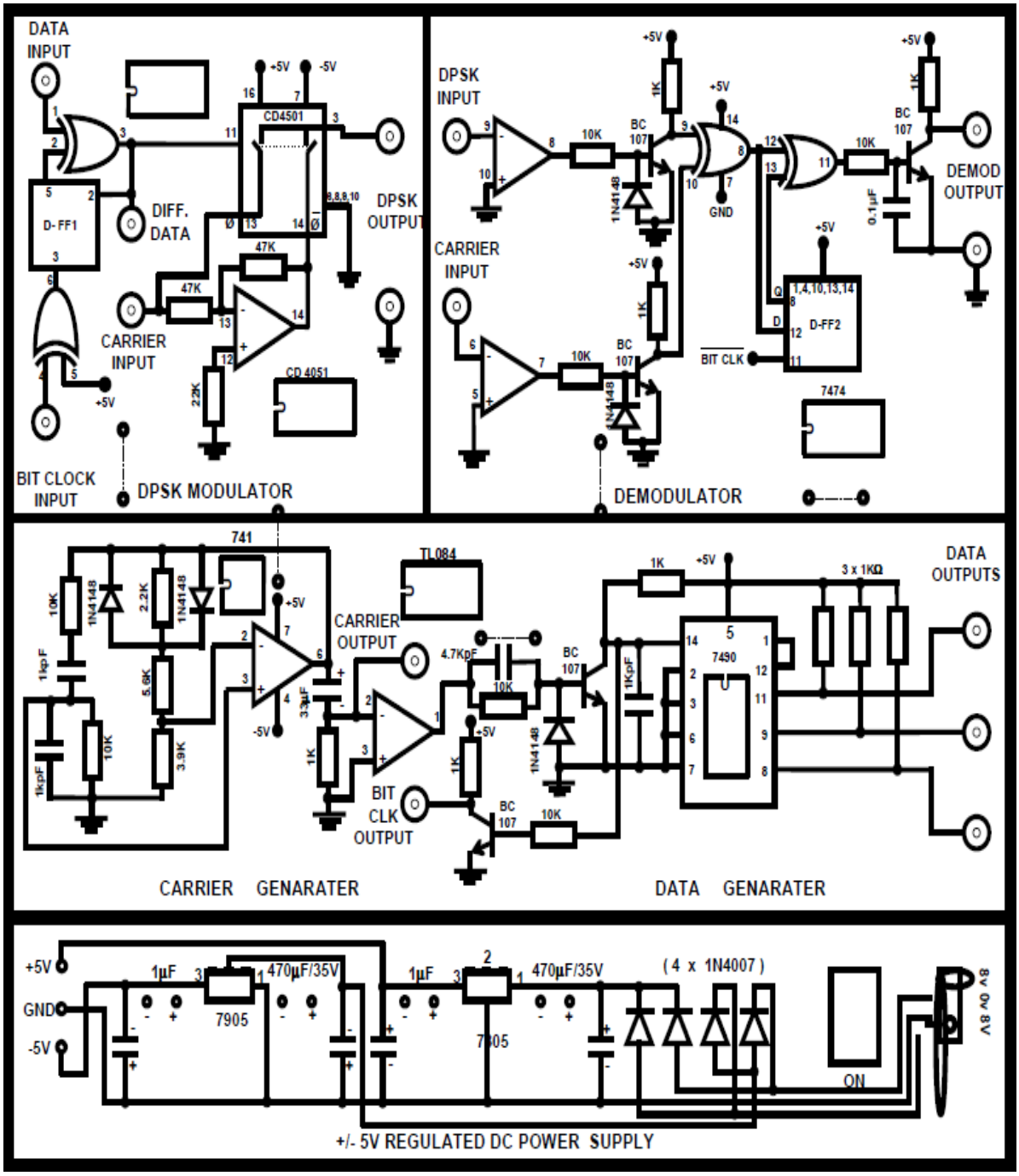
THEORY

The carrier wave signal is generated by a wein bridge oscillator around *** KHz at ±5V P-P sine wave using 741 the sine wave is convert into square wave using TL084 in comparator mode. The Transistor BC 107 converts the square signal to TTL levels. This is used as a basic bit clock or 180^0 for a mark and 0^0 for space. This Square wave is used as a clock input to a decade counter (IC 7490) which generates the modulating data outputs.

MODULATION

The Differential signal to the modulating signal is generated using an Exclusive -OR gate (7486) and a 1-bit delay circuit using D Flip Flop 7474 (It is shown in fig-1). CD 4051 is an analog multiplexer to which carrier is applied with and without 180° degrees Phase shift (created by using an operational amplifier connected in inverting amplifier mode) to the input of the TL084. Differential signal generated by Ex-OR gate (IC7486) is given to the multiplexer's control signal input. Depending upon the level of the control signal, carrier signal applied with or without phase shift is steered to the output. 1-bit delay generation of differential signal to the input is created by using a D-flip-flop(IC7474).

Circuit diagram:



DEMODULATION

During the demodulation, the data and carrier are recovered through a TL084 op amp in comparator mode . This level is brought to TTL level using a transistor and is applied to one input of an EX-OR gate. To the second input of the gate, carrier signal is applied after conversion into a +5V signal. So the EX-OR gate output is equivalent to the differential signal of the modulating data. This differential data is applied to one input of an Exclusive -OR gate and to the second input, after 1-bit delay the same signal is given. So the output of this Ex-OR gate is the recovered Modulating signal.

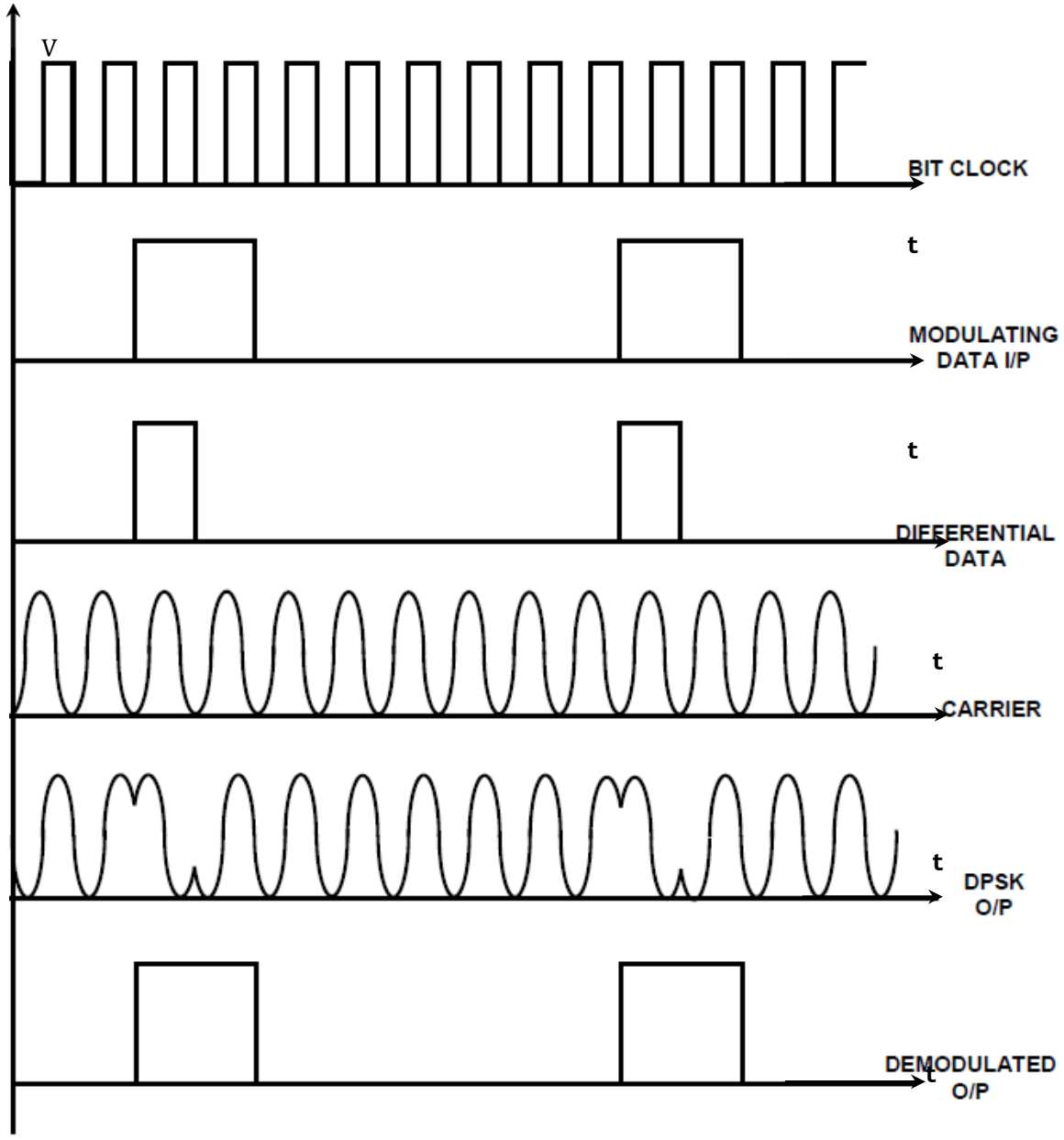
HARD WARE SPECIFICATIONS

1. Panel lay out diagram with components mounted on PCB /Panel
2. Built in variable DC power supplies +/ - 5V ,-350mA, the figures given.
3. ICs 741, 7490, 7474, CD4051, 7486 are provided on the trainer and the hardware details are given.
4. User Manual
5. Set of patch chords

6.EXPERIMENTAL PROCEDURE

1. 'Switch ON' the experimental board.
2. Check the carrier signal and the data generator signals initially.
3. Apply the carrier signal to the carrier input of the DPSK modulator and give the data generator to the data input of DPSK modulator and bit clock output to the input of DPSK modulator and Bit Clk O/P to Bit Clk input of modulator.
4. Observe the DPSK modulating output with respect to the input data generator signal of dual trace oscilloscope (observe the DPSK modulating signal on channel 1and the data generator signal on channel 2), and observe the DPSK Signal with respective to Differential data also.
5. Give the output of the DPSK modulator signal to the input of demodulator, give the bit clock output to the bit clock input to the demodulator and also give the carrier output to the carrier input of demodulator.
6. Observe the demodulator output with respect to data generator signal (modulating signal)

Model waveforms:



DPSK Signal Waveforms

PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

Result:

Thus the DPSK modulation and demodulation is performed and graphs were plotted.

5. Folded Dipole Antennas

Aim: To study folded dipole antenna and to calculate beam-width, front /back ratio, and gain of the antenna.

Apparatus Required:

1. Folded dipole Antenna
2. Detector
3. Connecting wires
4. Power supply

Theory

A folded dipole is a dipole antenna, with the ends folded back around and connected to each other, forming a loop as shown in Figure 1.

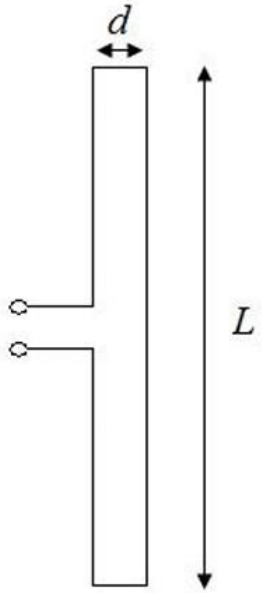


Figure . Folded dipole of length *L*.

Typically, the width *d* of the folded dipole is much smaller than the length *L*.

Because the dipole is a closed loop, one would expect the input impedance to depend on the input impedance of a short-circuited transmission line of length *L* (although unfortunately it depends on a transmission line of length *L*/2, which doesn't quite make intuitive sense to me). Also, because the dipole is folded back on itself, the currents can reinforce each other instead of cancelling each other out, so the input impedance will also depend on the impedance of a dipole antenna of length *L*.

Letting Zd represent the impedance of a dipole antenna and Zt represent the transmission line impedance given by:

$$Z_t = jZ_0 \tan\frac{\beta L}{2}$$

The input impedance ZA of the folded dipole is given by:

$$Z_A = \frac{4Z_t Z_d}{Z_t + 2Z_d}$$

The folded dipole is resonant and radiates well at odd integer multiples of a half-wavelength (0.5 λ , 1.5 λ , ...). The input impedance is higher than that for a regular dipole.

The antenna impedance for a half-wavelength folded dipole antenna can be found from the above equation for ZA; the result is ZA=4*Zd. At resonance, the impedance of a half-wave dipole antenna is approximately 70 Ohms, so that the input impedance for a half-wave folded dipole is roughly 280 Ohms.

Because the characteristic impedance of twin-lead transmission lines are roughly 300 Ohms, this dipole is often used when connecting to this type of line, for optimal power transfer.

The radiation pattern of half-wavelength folded dipoles have the same form as that of half-wavelength dipoles.

PROCEDURE

1. Arrange the setup as given in the block diagram
2. Mount folded dipole antenna on the transmitter mask
3. Bring the detector assembly near to main and adjust the height of both transmitting and receiving antenna
4. Keep Detector assembly away from the main unit approximately 1.5 meter and align both of them .Ensure that there is no reflector sort things in the vicinity of the experiment such as a steel structure ,pipes, cables etc.
5. Keep the RF level and FS adjust to minimum and unidirectional coupler switch to FWD(Forward adjustment knob).
6. Keep detector level control in the centre approximately
7. Increase RF level gradually and see that there is deflection in the detector meter
8. Adjust RF level and detector level, so that the deflection in detector meter is approximately 30-35mA.
9. Align arrow mark on the disk with zero of the goniometer scale
10. Start taking the reading at the interval of 10 degree, and note the deflection on the detector assembly.
11. Using conversion chart convert mA readings into db.
12. Plot the polar graph in degrees of rotation of antenna against level in the detector in dBs

Tabulation:

S.No	Angle in Degrees	Detector reading(mA)	Gain in dB

Result:

6. BINARY PHASE SHIFT KEYING

AIM:-

To plot the wave form for Binary Phase Shift Keying signal (BPSK) using MATLAB for a stream of bits.

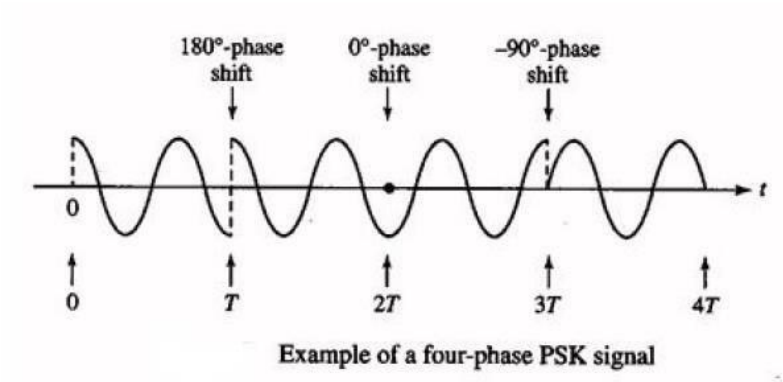
THEORY:-

In carrier-phase modulation, the information that is transmitted over a communication channel is impressed on the phase of the carrier. Science the range of the carrier phase is $0 \leq \theta \leq 2\Pi$,the carrier phases used to transmit digital information via digital-phase modulation are $\theta_m=2\Pi m/M$, for m=0,1,2…..,M-1.Thus for binary phase modulation(M=2),the two carrier phase are $\theta_0 =0$ and $\theta_1 = \Pi$ radian. For M-array phase modulation=2^k, where k is the number of information bits per transmitted symbol.

The general representation of a set of M carrier-phase-modulated signal waveforms is

$u_m(t) = AgT(t) \cos(2\Pi fct+2\Pi m/M)$, m=0,1,…….,M-1

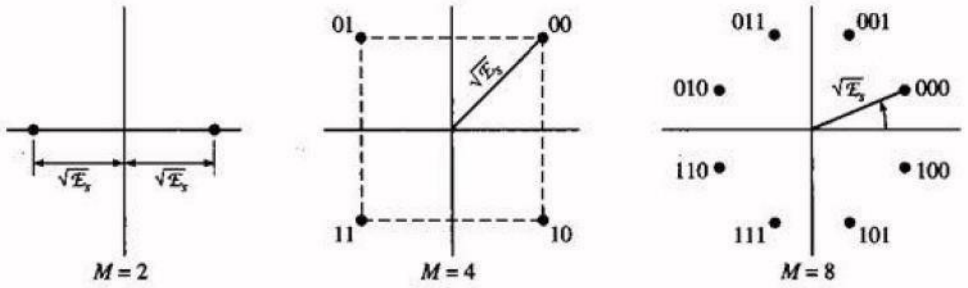
Where, gT(t) is the transmitting filter pulse shape, which determines the spectral characteristics of the transmitted signal, and A is the signal amplitude. This type of digital phase modulation is called phase-shift-keying.



Example of a four-phase PSK signal

Signal point constellations for M=2, 4 and 8 are illustrated in figure. We observe that binary phase modulation is identical to binary PAM (binary antipodal signals).The mapping or assignment, of k information bits into the M= 2^k possible phases may be done in a number of ways. The preferred assignment is to Gray in coding, in which adjacent phases differ by one binary digit, as illustrated

below in the figure. Consequently, only a single bit error occurs in the k-bit sequence with Gray encoding when noise causes the incorrect selection of an adjacent phase to the transmitted phase



PSK signal constellations

In figure shows that, block diagram of M=4 PSK system. The uniform random number generator fed to the 4-PSK mapper and also fed to the compare. The 4-PSK mapper split up into two phases. On the other hand, Gaussian RNG adds to the modulator. The two phases are fed to the detector. The output goes to the compare. The Uniform random number generator and detector also fed to the detector and finally fed to the bit-error counter and symbol-error counter.

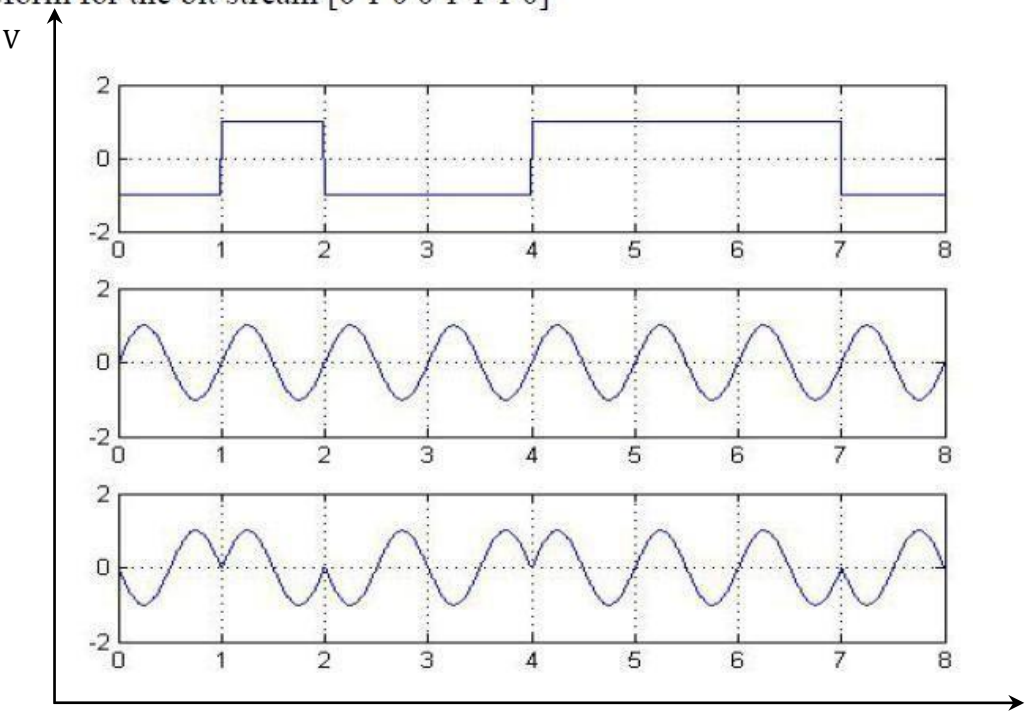
MATLAB PROGRAM:-

```
clear;
clc;
b = input('Enter the Bit stream \n ');          %b = [0 1 0 1 1 1 0];
n = length(b);
t = 0:.01:n;
x = 1:1:(n+1)*100;
for i = 1:n
   if (b(i) == 0)
      b_p(i) = -1;
   else
      b_p(i) = 1;
   end
   for j = i:.1:i+1
      bw(x(i*100:(i+1)*100)) = b_p(i);
   end
end
```

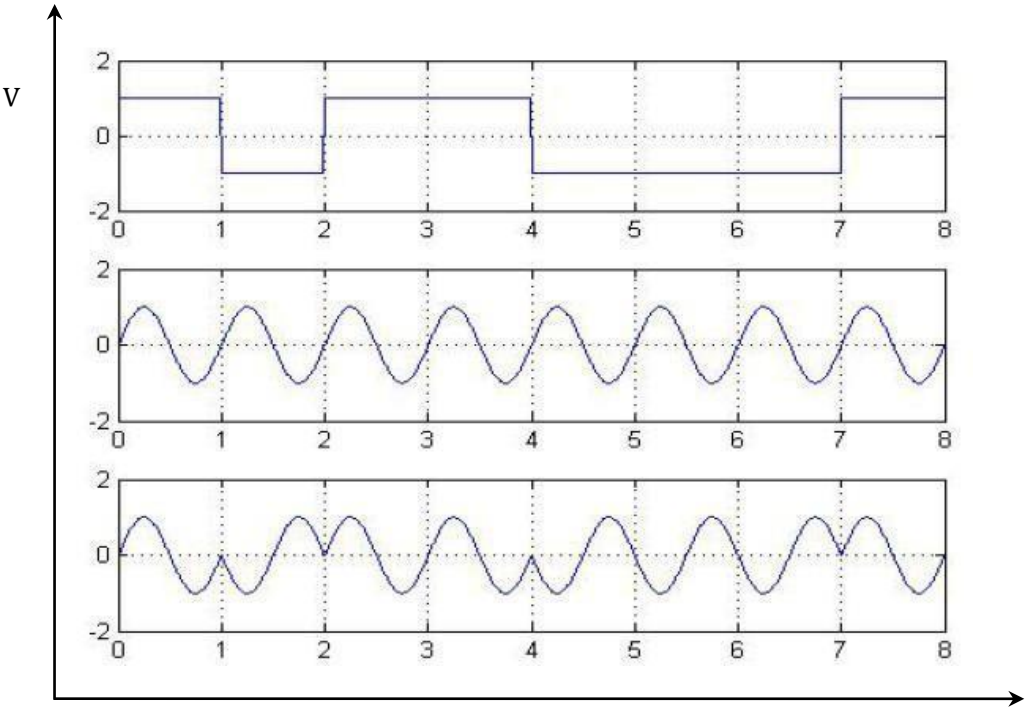
```
bw = bw(100:end);
sint = sin(2*pi*t);
st = bw.*sint;
subplot(3,1,1)
plot(t,bw)
grid on ; axis([0 n -2 +2])
subplot(3,1,2)
plot(t,sint)
grid on ; axis([0 n -2 +2])
subplot(3,1,3)
plot(t,st)
grid on ; axis([0 n -2 +2])
```

OBSERVATION:-

Output waveform for the bit stream [0 1 0 0 1 1 1 0]



Output waveform for the bit stream [1 0 1 1 0 0 0 1]



Result: The program for BPSK modulation and demodulation has been simulated.

7. QPSK MODULATION & DEMODULATION

Aim: To generate a QPSK modulated signal for the given input data and its demodulated signal.

INTRODUCTION & THEORY:

For Transmission of Digital signal over limited band width channel various methods of Modulation techniques were developed from simple FSK, PSK system to complex DPSK, DASK and QPSK system. In simple PSK system, the phase of the carrier was modulated such that the carrier phase was reversed during the logic zero bit (f_c =180^0) while the carrier without any phase shift (f_c=0) was transmitted during the logic "1" level or vice versa. This method is also known a BPSK or Bi phase shift keying. If f_d is the data rate, then the band width required for transmitting BPSK signal would be $2f_d$.

In QPSK, the phase of the carrier depends upon the pair of successive bits in the data stream. Thus, there are four possible combinations of bit pair viz 00, 01,10, and 11.
During each combination of bit pair the carrier frequency f_c is transmitted with quadrature phase difference as shown below in Table 1.

TABLE –1

Bit Pair	Phase of Carrier
00	fc $\angle 0^0$
01	fc $\angle 90^0$
10	fc $\angle 180^0$
11	fc $\angle 270^0$

Bit pair & corresponding carrier

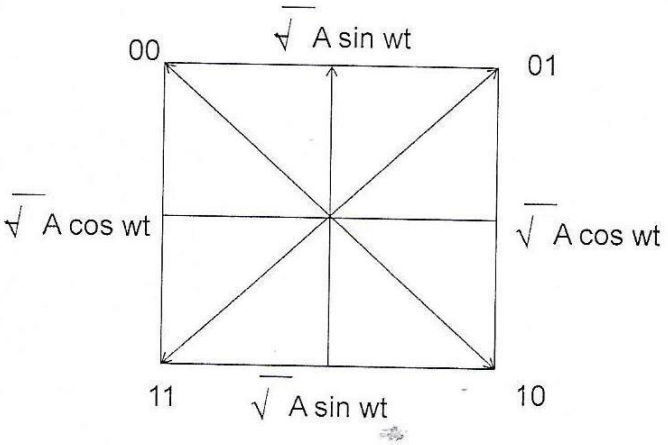


Fig 1: Phase diagram of carrier

The theoretical generation of QPSK is shown in the fig.1

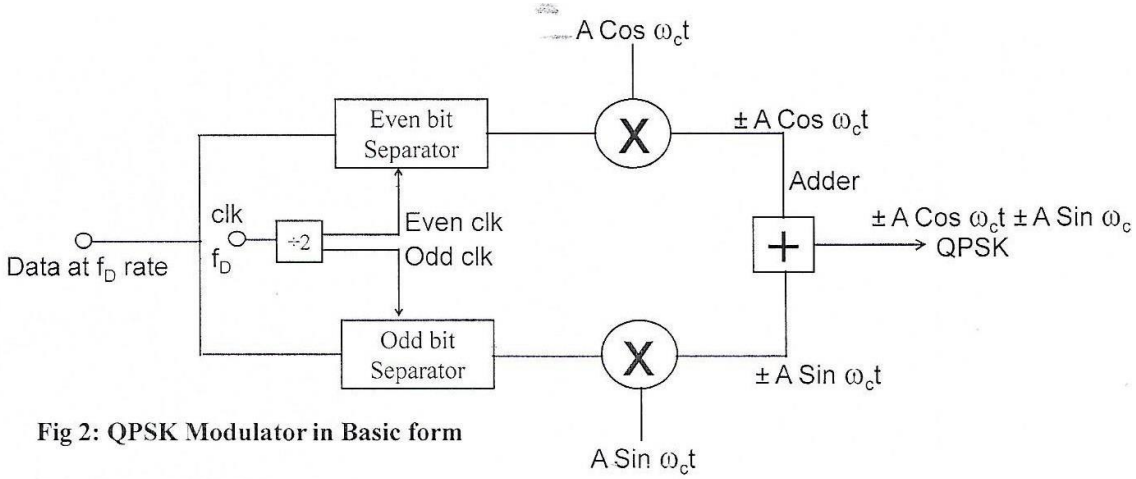


Fig 2: QPSK Modulator in Basic form

Principle of QPSK Generation:

The data coming at the rate of f_D the basic form of a QPSK Modulator is shown in Fig 2 is given to odd and even bit separators which are nothing but D Flip Flop driven by even clock and odd clock. The even clock and odd clock are generated by a toggle flip flop. The even and odd bit stream are generated at the rate of $f_D/2$.

This bit streams modulates the corresponding carrier A sin wt and A cos wt such that a phase shift of 180^0 is introduced for a logic '1' level as against logic 'O' level.

The adder gives the algebric sum of the modulated components. We observe from the Fig 1. phase diagram that, the resultant wave forms again will have 90^0 phase difference from successive bit pairs. It may also be noticed that succeeding bit pair will have only one bit change resulting only in $\pm 90^0$ phase shift of the resulting summer output.

In actual practice the quadriphase carriers can be generated and switched digitally depending upon the bit pair combination.

QPSK Receiver:

At the receiver end, the process of demodulation involves QPSK signal is modulated (using Balanced Modulation) again using recovered carrier signals (Cos ω_ct and Sin ω_ct). The resulting dual outputs are integrated to generate DC logic levels, of bit pairs. They are converted from parallel to serial signals by using time division switching.

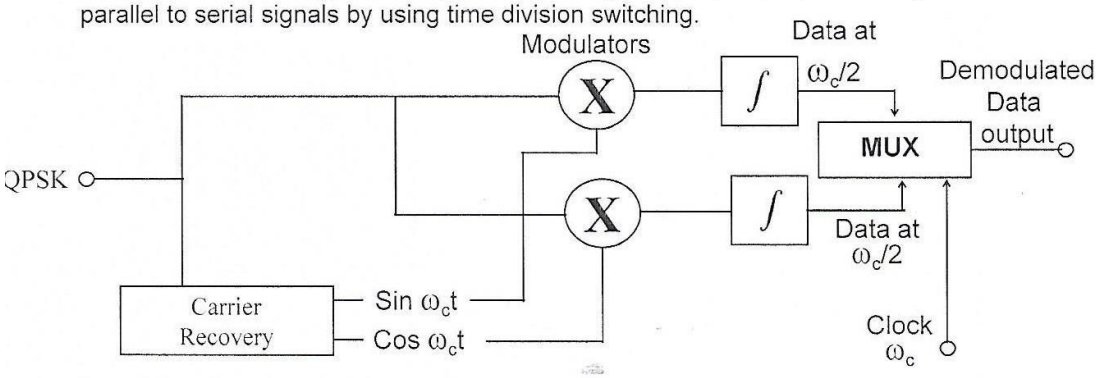
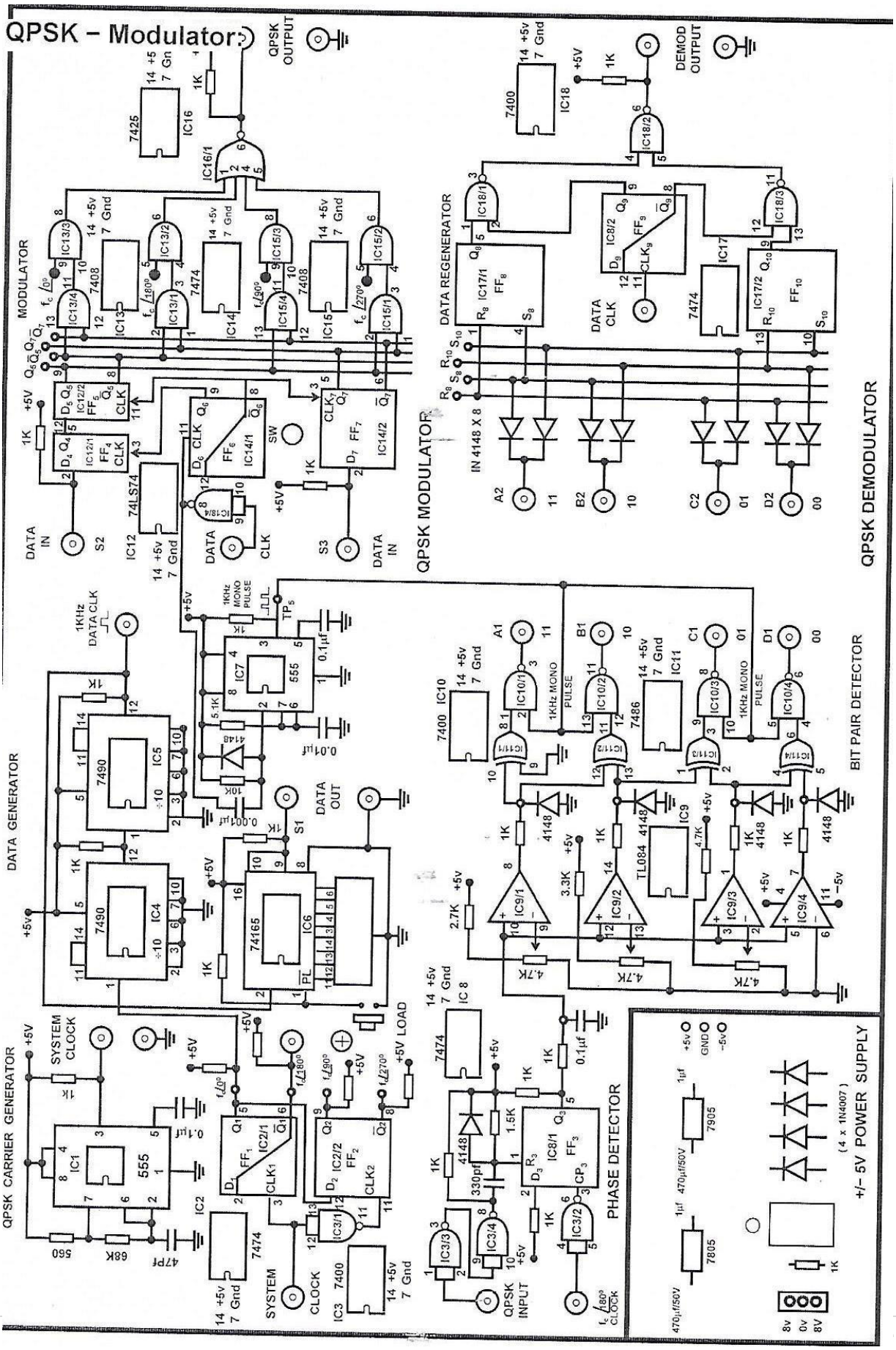


Fig3 : A QPSK receiver in basic form.


QPSK – Modulator:
QPSK MODULATOR
QPSK DEMODULATOR
MODULATOR
DATA REGENERATOR
DATA GENERATOR
BIT PAIR DETECTOR
QPSK CARRIER GENERATOR
PHASE DETECTOR
+/- 5V POWER SUPPLY
QPSK OUTPUT
DEMOD OUTPUT
DATA IN
DATA OUT
DATA CLK
SYSTEM CLOCK
QPSK INPUT
+5V LOAD
IN 4148 X 8
1KHz MONO PULSE
TL084
74LS74
7400
7408
7474
7486
7490
7425
74165
555

Refer to the QPSK Modulator circuit diagram shown in Fig.4. The 555 timer circuit generates system clock a square wave frequency of approximately 200kHz. The quadri phase carriers $f_c \angle 0^0$, $f_c \angle 90^0$, $f_c \angle 180^0$ & $f_c \angle 270^0$ at approximately 100kHz are generates by two D – Flip Flops DFF1 & DFF2. These four carrier signals are given to four AND gates which are exclusively enabled by the presence of bit pair combination in the Data. The carrier switching with respect to the bit pair is shown in the table 2 below.

Table – 2

Bit pair b0b1	Carrier selected
00	fc $\angle 0^0$
01	fc $\angle 90^0$
10	fc $\angle 180^0$
11	fc $\angle 270^0$

The four AND gate outputs are 'OR' ed using a 4–input NOR gate followed by a NAND inverter. The resulting output is a QPSK modulated signal.

The data stream is generated at approx. 1kbps rate using a synchronous1kHz clock derived from 100kHz by two divide by 10 (IC 7490x2) circuit and a shift register (IC 74165) with parallel load and serial shift facility.

QPSK–DEMODULATOR:

The practical QPSK de modulator is shown in shown in fig:5.

In this method, a phase detector is employed to find the instantaneous phase of the QPSK signal with respect to a carrier clock $f_c \angle 180^0$. This consists of a D Flip Flop with $f_c \angle 180^0$ clock at the Clock Input and QPSK signal at the Reset input. Depending upon the negative going edge of the QPSK signal the D Flip Flop Resets Q to zero, while the positive edge at clk input R resets Q to 1 level as 'D' is pulled up to '1' level. Thus a series of pulses occur at the output of the D Flip Flop which are integrated using an RC Filter. The DC output available at the output of RC filter with respect to phase difference in the signals f_c 80^0 clk and QPSK signal is shown in Table 3.

Phase difference	Integrated DC output (Approx)	Corresponding transmitted bit fair combination
$\angle 0^0$	0.2V	00
$\angle 90^0$	1V	01
$\angle 180^0$	1.8V	10
$\angle 270^0$	3.0V	11

Table 3 : Output voltage Vs Phase of the carrier in QPSK with respect to the f_c 180^0 clock

The output of the phase detector and the corresponding Bit pair combination that generated the phase shift of the carrier is shown in Table 3. Therefore this bit pair combination is to be regenerated at the receiver before the serial data could be re constructed. For this purpose four comparators with different reference levels are provided. Their outputs are normalised to TTL levels using a resistance and clamping diode combination. Through a set of Four EX-NOR (EX-OR plus INV) gates pulses are generated in the respective phase periods of the carrier. The differentiated leading negative edges are used to appropriately 'Set' or 'Reset' two RS – Flip Flops (7474) which gives the bit pair information. This parallel Bit Pair information is transferred into serial bit pair (Referenced Data) using three NAND gates. The QPSK input is thus demodulated to reconstruct digital serial data.

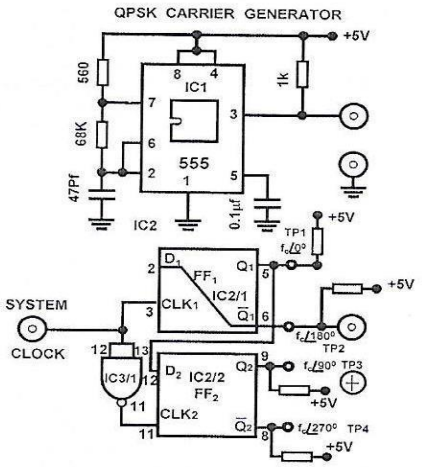
Experimental Procedure:

1. Connect the QPSK Modulator -- Demodulator to Mains chord to AC source and switch on the trainer.
2. Check the phase difference of the Quadri Phase carries generated at the outputs of FFI and FF2.

Connect the output at TP1 to channel 1 of oscilloscope and synchronise the scope with channel1 and positive slope trigger.

Observe on channel 2 the phase shifted carriers at TP2, TP3 and TP4 w.r.t the carrier at TP1 and fill up the Table.

Signal at	Phase angle w.r.t Carrier at TP1
TP1	$\angle 0^0$
TP3	$\angle 90^0$
TP2	$\angle 180^0$
TP4	$\angle 270^0$



able 4: Qudriphase carrier – phase angle differencier

2. Test the odd even bit separator for static bit levels.

The logic levels at socket S2 and S3 will determine the odd bit and even bit in the Data stream. Test the following Bit stream combinations as given in Table 5..

Note: S2 or S3 when open presents a Logic 1 level as the inputs are pulled up.

3. Test the selection of carriers w.r.t. the bit pair generation.
Observe on channel 1 carrier fc $\angle 180^0$ at TP1 connect on channel 2 the output of QPSK Modulator, observe the switched carrier as shown in Table 4.

TABLE 5

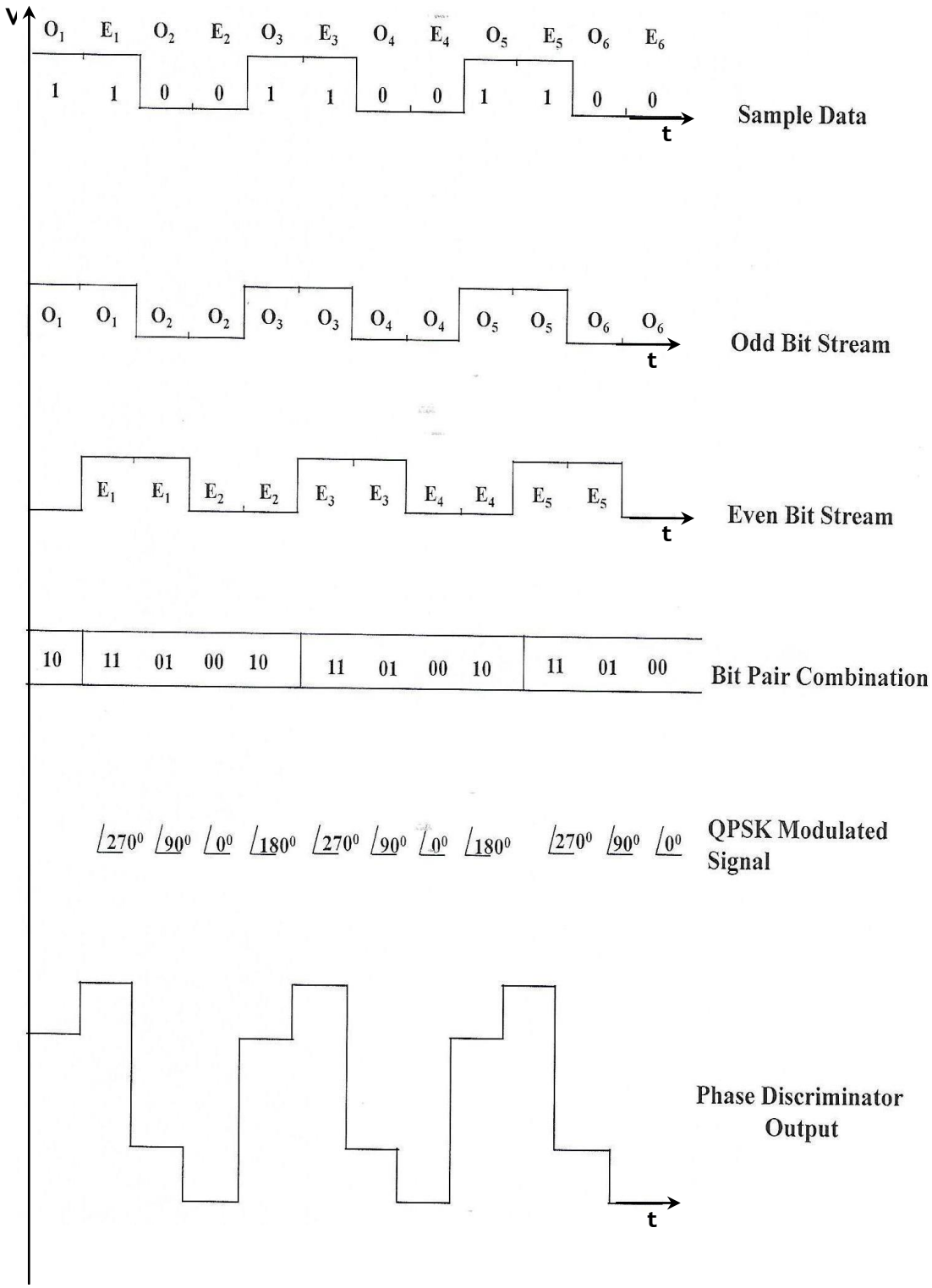
Socket S2	Socket S3	Phase angle of QPSK output w.r.t fc $\angle 180^0$ carrier on channel1
Gnd (0)	Gnd(0)	$f_c \angle 0^0$
Open (1)	Gnd (0)	$f_c \angle 180^0$
Gnd (0)	Open (1)	$f_c \angle 90^0$
Open (1)	Open (1)	$f_c \angle 270^0$

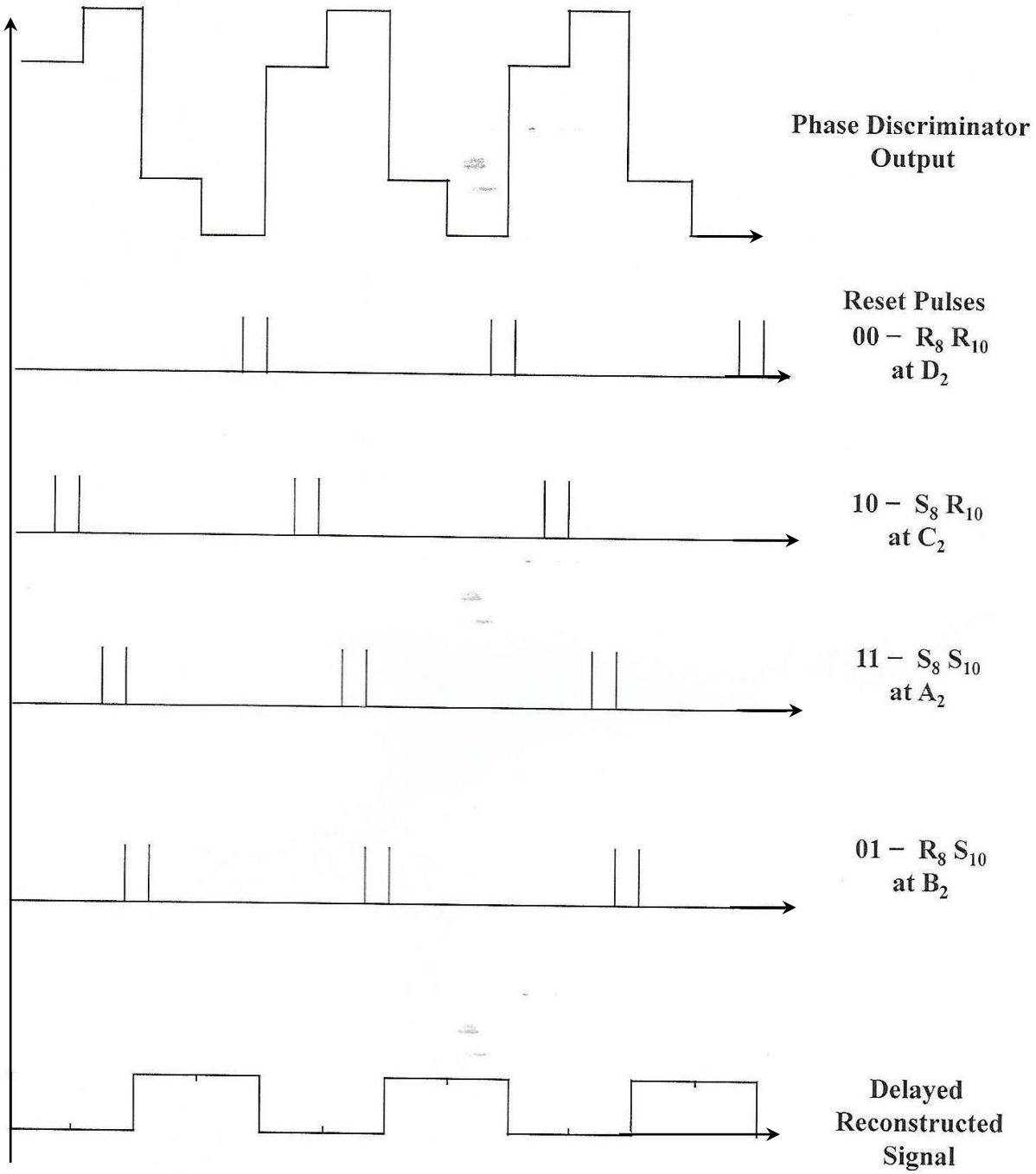
Table 6: Phase angle of carrier switched corresponding to the bit pair input

QPSK DEMODULATOR :

1. Connect QPSK output to the QPSK input and fc $\angle 180^0$ carrier at Clock input of Phase detector.
2. Observe phase detector output at Channel 1.
3. Connect bit pair detector output on Channel 2. We can observe small pulses corresponding to each bit pair combinations i.e., 11,10, 01 & 00 at A1, B1, C1 & D1 respectively. These pulses indicate no. of particular bit pair combinations for the selected 8−bit word.
4. Connect bit pair detector to data regenerator i.e A1 to A2; B1 to B2; C1 to C2 & D1 to D2. And data clock at clock input.
5. The output of data regenerator is the demodulated signal.

   (Note: This is the delayed output, because we have introduced one bit delay in the Modulator)


V
O1 E1 O2 E2 O3 E3 O4 E4 O5 E5 O6 E6
1 1 0 0 1 1 0 0 1 1 0 0
t
Sample Data
O1 O1 O2 O2 O3 O3 O4 O4 O5 O5 O6 O6
t
Odd Bit Stream
E1 E1 E2 E2 E3 E3 E4 E4 E5 E5
t
Even Bit Stream
10 11 01 00 10 11 01 00 10 11 01 00
Bit Pair Combination
270⁰ 90⁰ 0⁰ 180⁰ 270⁰ 90⁰ 0⁰ 180⁰ 270⁰ 90⁰ 0⁰
QPSK Modulated Signal
t
Phase Discriminator Output



Note : A Toggle Switch S is Provided to interchange Q6 and $\overline{Q6}$ so that proper initialization is done for modulation. If the output of the phase detector is improper change the switch position S to the other side.

Result: Thus the QPSK modulated signal is generated and it is demodulated.

8. DELTAMODULATION

AIM

To study the Delta Modulation process by comparing the present signal with the previous signal of the given Modulating signal.

INTRODUCTION

In radio transmission, it is necessary to send audio signal (e.g. Music, speech etc.) from a broad casting station over great distances to a receiver. This communication of audio signal which does not employ any wire and is sometimes called wireless. The audio signal cannot be sent directly over the air for appreciable distance. Even if the audio signal is converted into electrical signal, the latter cannot be sent very far without employing large amount of power. The energy of a wave is directly proportional to its frequency. At audio frequencies (20Hz to 20KHz), the signal power is quite small and radiation is not practicable.

The radiation of electrical energy is practicable only at high frequencies e.g. Above 20KHz. The high frequency signals can be sent thousands of miles even with comparatively small power. Therefore, if audio signal is to be transmitted properly, some means must be devised which will permit transmission to occur at high frequencies while it simultaneously allows the carrying of audio signal . This is achieved by imposing electrical audio signal on high frequency carrier/ The resultant waves are known as modulated waves or radio waves and the process is called modulation. At the radio receiver, the audio signal is extracted from the modulated wave by the process is called modulation. At the radio receiver, the audio signal is extracted from the modulated wave by the process called demodulation. The signal is then amplified and reproduced into sound by the loudspeaker.

MODULATION

A high frequency carrier wave is used to carry the audio signal which is done by changing some characteristic of carrier wave in accordance with the signal. Under such conditions, the audio signal will be contained in the resultant wave. The process is called modulation and defined as " The process of changing some characteristic (e.g. Amplitude, Frequency or Phase) of a carrier wave in accordance with the intensity of the signal is known as Modulation".

Modulation means to "change". In modulation, some characteristic of a carrier wave is changed in accordance with the intensity (I.e. Amplitude) of the signal. The resultant wave is called modulated wave or radio wave and contains the audio signal. Therefore, modulation permits the transmission to occur at high frequency while it simultaneously allows the carrying of the audio signal.

NEED FOR MODULATION

Modulation is extremely necessary in communication system due to the following reasons.

1. PRACTICAL ANTENNA LENTH : In order to transmit a wave effectively, the length of the transmitting antenna should be approximately equal to the wavelength of the wave.

$$\text{Now} \quad \text{Wavelength} = \frac{\text{Velocity}}{\text{frequency}} = \frac{3 \times 10^8}{\text{frequency (Hz)}} \text{ meters}$$

As the audio frequencies range from 20Hz to 20KHz, therefore, if they are transmitted directly into space, the length of the transmitting antenna required would be extremely large. For instance, to radiate a frequency of 20KHz directly into space, we would need an antenna length of $3 \times 10^8 \setminus 20 \times 10^3 = 15{,}000$ meters. This is too long antenna to be constructed practically. For this reason, it is impracticable to radiate audio signal directly into space. On the other hand, if a carrier wave say of 1000KHz is used to carry the signal, we need an antenna length of 300 meters only and this size can be easily constructed.

2. OPERATING RANGE

The energy of a wave depends upon its frequency. The greater the frequency of the wave, the greater the energy possessed by it. As the audio signal frequencies are small, therefore these cannot be transmitted over large distances if radiated directly into space. The only practical solution is to modulate a high frequency carrier wave with audio signal and permit the transmission to occur at this high frequency (I.e carrier frequency).

3. WIRELESS COMMUNICATION

One desirable feature of radio transmission is that it should be carried without wires I.e. Radiated into space. At audio frequencies radiation is not practicable because the efficiency of radiation is poor. However, efficient radiation of electrical energy is possible at high frequencies. For this reason, modulation is always employed in communication systems.

INTRODUCTION

Delta Modulation is a Differential Pulse Code Modulation Technique, in which the difference signal between two successive samples is encoded into a single bit code.

Circuit Diagram:

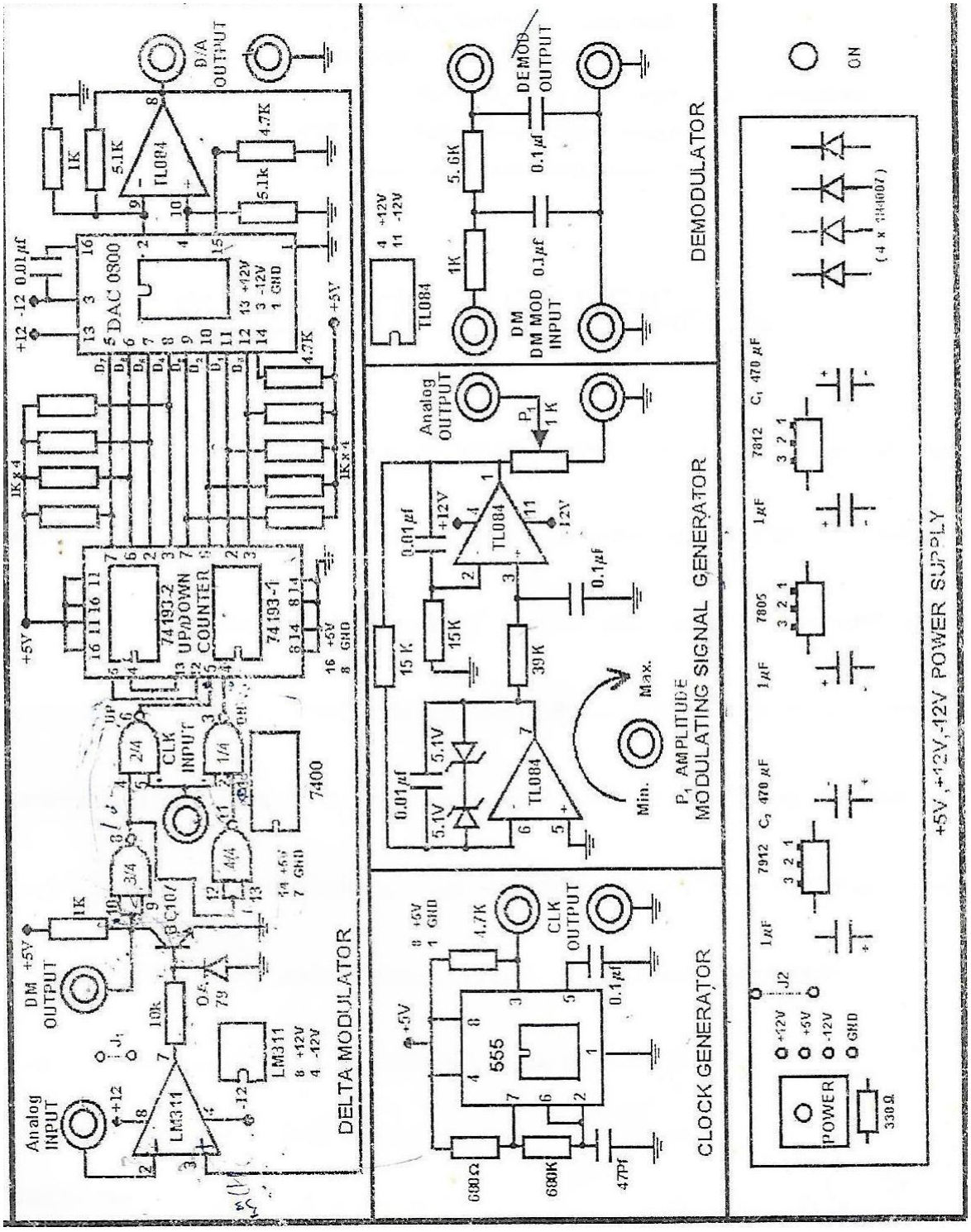


Fig-1 shows the block diagram of the Delta Modulation. This is also known as Linear Delta Modulator. The signal m(t) is the analog input signal. While r(t) is a reconstructed signal which is same as the quantised input signal with 1 bit delay. The signal r(t) tries to follow the input signal m(t) with one bit period delay.

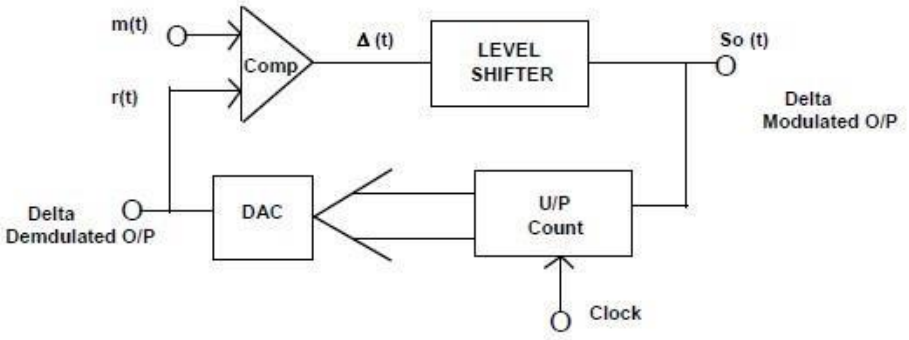


FIG - 1 BLOCK DIAGRAM OF DELTA MODULATION

THEORY

The process of encoding is as follows. The comparator compares the input signal m(t) and r(t). If m(t) > r(t) a logic 1 is generated at the output of the comparator, otherwise a logic 0 is generated.The value of logic 1 or logic 0 turmed as Δ(t) is held for the bit duration by the sample and hold current to generate So (t), the Delta Modulated Output.

This output So(t) is fed to the 8 bit binary up/down counter to control it's count direction. A logic 1 at the mode control input increases the count value by one and a logic '0' decrements the count value by one . All the 8 outputs of the counter are given to DAC to reconstruct the original signal. In essence the counter & Decoder forms the Delta Modulator in the feedback loop of the comparator. Thus, if the input signal is higher than the reconstructed signal the counter increments at each step so as to enable the DAC output to reach to the input signal values. Similarly if the input signal m(t) is lower than the reconstructed signal r(t), the counter decrements at each step, and the DAC output gets reduced to reach a value to that of m(t).

The block diagram of Delta demodulator is shown below. It works in the same way as it was in the feedback loop of the Delta modulator. The received Delta modulated signal So(t) is given to the mode control input (U/ D) of the up/ down counter. The counter is 8 bit wide and counts in binary fashion. All the 8 outputs are connected to an 8 bit DAC which gives a quantised analog signal (stepped waveform). A low pass filter is used to smooth out the steps. A buffer amplifier provides the necessary drive capability to the output signal. Thus the digital Delta modulated data is demodulated and reconstructed into an analog signal.

Although this process of Delta Modulation and Demodulation is a simple and cost effective method of coding, there will be poor approximation at starting buildup and ' hunting' at flat top signals.

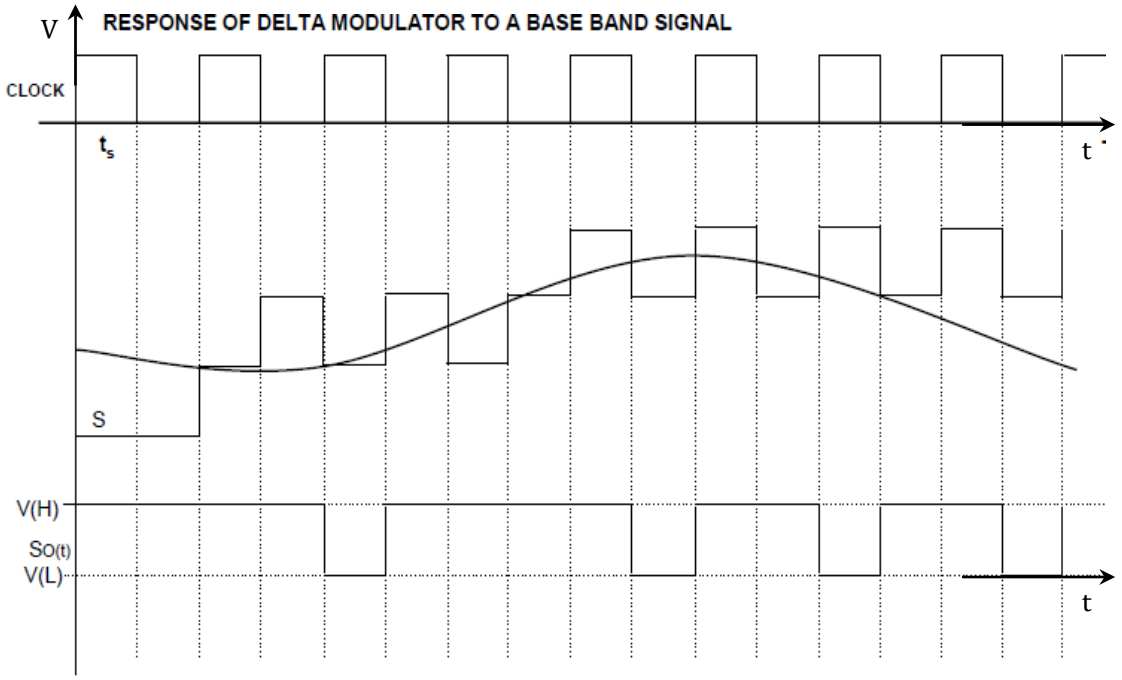


Fig - 2

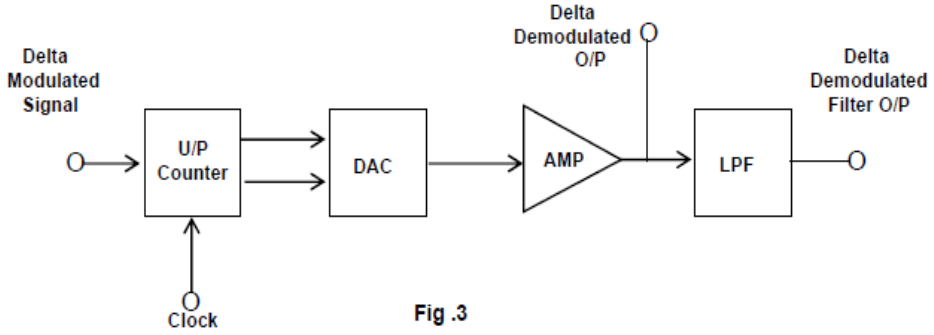


Fig .3

RESPONSE LIMITATIONS OF DELTA MODULATION

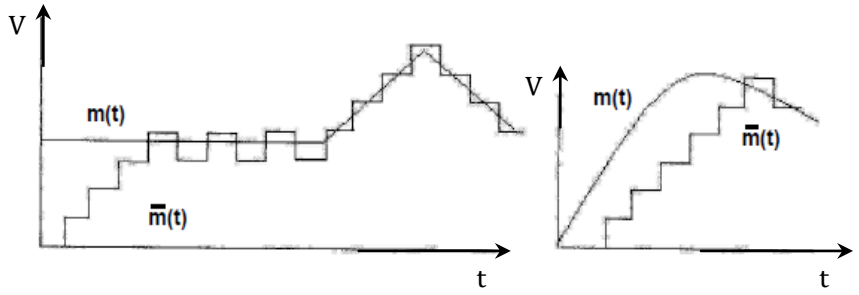


Fig .4

Another limitation in Delta Modulation is ' slope overloading;. Basically the DAC can produce a Max. signal variation of (256x 5) volts in 256 clock pulses where is the quantisation step size T_c is the clock period the max. Slope that the DAC can produce in S/ T_s volts / second which is the limiting factor where S is the step size and t_s is clock period. If the input signal slope is higher than this or in other words, if the input signal frequency is greater than the limiting value, slope overloading occurs. In such a case true reproduction of the analog signal is not possible. A sinusoidal waveform of amplitude A & frequency f has a maximum slope of $2\Delta fA$ which occurs at zero crossing of the sine wave. If the overloading is to be avoided then the following condition should be satisfied.

$$S_f > / 2\pi fA$$

When S = quantisation step size,
f_s = sampling frequency (Bit frequency), f = Signal frequency , A = Signal Amplitude

$$f_s = \frac{2\pi fA}{S} = \frac{\pi f2A}{S}$$

When 2A = Peak to Peak Amplitude
= 256 X s = DAC Max. Amplitude
$f_s = \pi f\ 256 = 256\ \pi f$

For a signal frequency of 200Hz, the sampling frequency should be
$f_s = 256\ X\ \pi\ X\ 200 = 160KHz$

HARDWARE SPECIFICATIONS

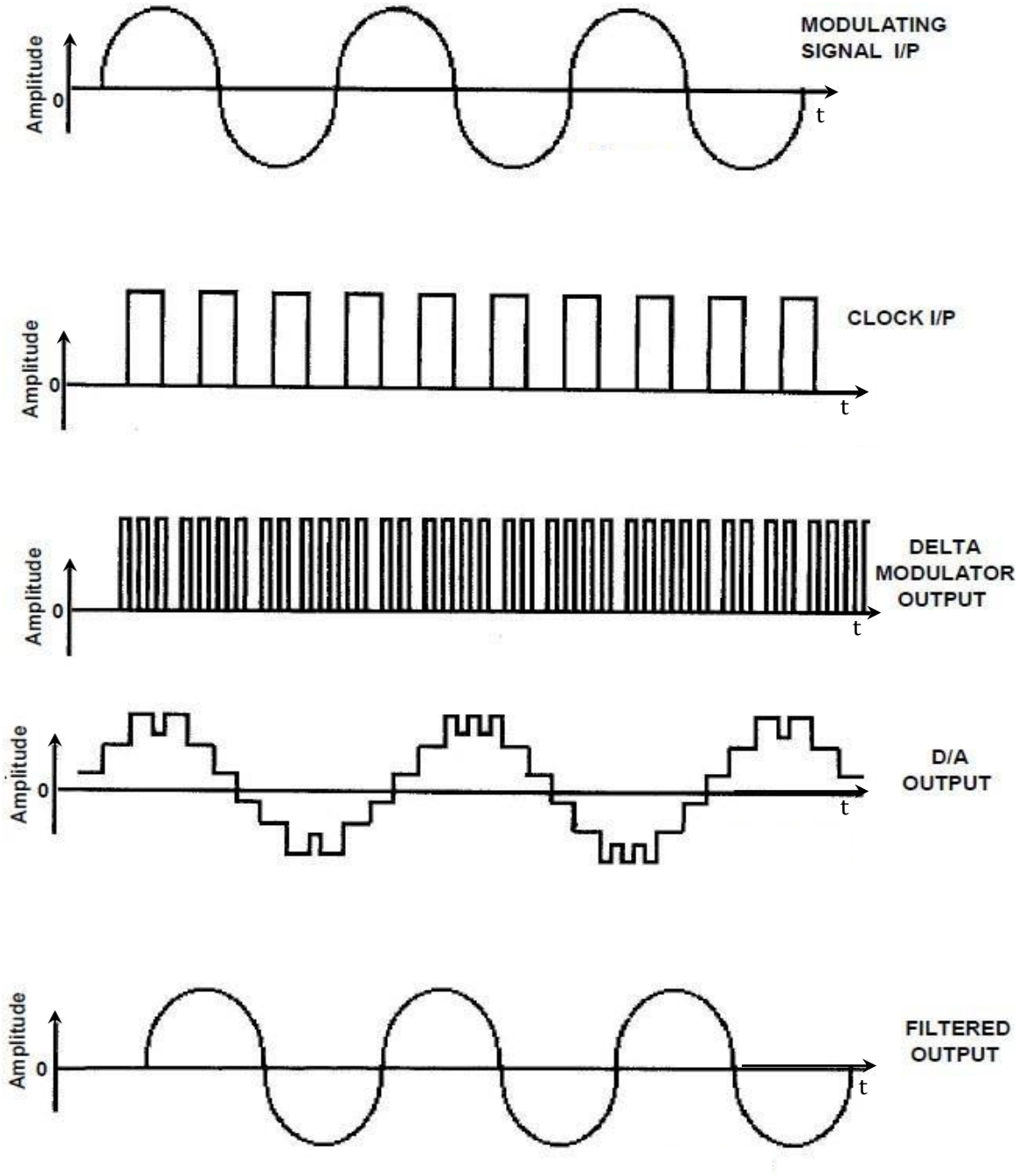
1. Delta Modulation and Demodulation Trainer.
2. Built in DC power supply + 5V / 350mA , +/- 12V / 350mA.
3. Provided with 2mm Sockets.
4. The ICs provided on the board are TL084(1No), 555 (1No), (74193 (2 Nos), DAC0800(1 No) , 7400 (1 No) , LM 311 (1 No).
5. Set of Patch chords Stackable 2mm - 6 Nos.
6. User Manual.

EXPERIMENTAL PROCEDURE

1. Connect the AC Adaptor to the mains and the other side to the Experimental Trainer.
2. Switch ON the experimental board.
3. Connect Clock Signal to the Delta Modulator circuit.
4. Connect Modulating Signal to the Modulating signal input of the Delta Modulator and observe the same on channel 1 of a Dual Trace Oscilloscope.
5. Observe the Delta Modulator output on channel II.
6. Connect this Delta Modulator output to the Demodulator.
7. Also connect the clock signal to the demodulator.
8. Observe the Demodulator output with and without RC filter on CRO.

MODELWAVEFORMS:

.



PRECAUTIONS:

1. Avoid loose and wrong connections.
2. Readings should be noted without parallax error.

RESULT: Thus Delta Modulated signal is generated for given input signal and it is demodulated.

9. LINEAR BLOCK CODE-ENCODER & DECODER

AIM: To Study the Hamming Code 7-bit Generation.

APPARATUS:

1. Linear Block Code-Encoder & Decoder Trainer Kit
2. 2mm Banana Cable
3. Regulated Power Supply

THEORY:

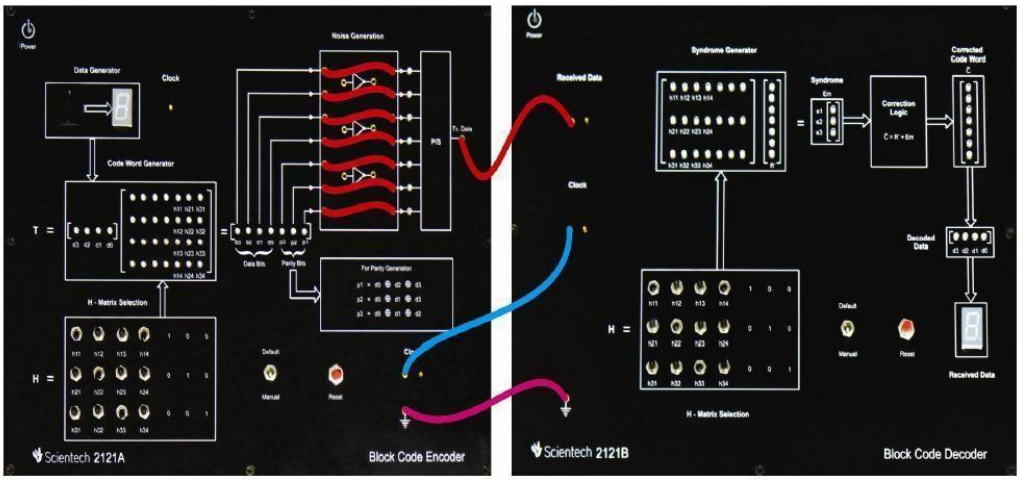
Error Detection and Correction:

Error detection is the ability to detect the presence of errors caused by noise or other impairments during transmission from the transmitter to the receiver. Error correction is the additional ability to reconstruct the original, error-free data. There are two basic ways to design the channel code and protocol for an error correcting system.

Linear block codes:

Linear block codes are conceptually simple codes that are basically an extension of single-bit parity check codes for error detection. A single-bit parity check code is one of the most common forms of detecting transmission errors. This code uses one extra bit in block of n data bits to indicate whether the number of 1s in a block is odd or even. Thus, if a single error occurs, either the parity bit is corrupted or the number of detected 1s in the information bit sequence will be different from the number used to compute the parity bit: in either case the parity bit will not correspond to the number of detected 1s in the information bit sequence, so the single error is detected. Linear block codes extend this notion by using a larger number of parity bits to either detect more than one error or correct for one or more errors. Unfortunately linear block codes, along with convolution codes, trade their error detection or correction capability for either and width expansion or a lower data rate, as will be discussed in more detail below. We will strict our attention to binary codes, where both the original information and the corresponding code consist of bits taking a value of either 0 or 1.

BLOCK DIAGRAM:



PROCEDURE:

1. Connect the power supply mains cord to the Scientech 2121Aand Scientech 2121B but do not turn ON the power supply until connections are made for this experiment.

2. Keep default/ manual switch in Manual mode.

3. There are some conditions regarding H-Matrix selection manually which are:
Any row should not be identically selected like there should not all 1's or all 0's.

Each row selection should be different from other row.

The matrix should be so chosen that all the rows are distinct and consist of at least three 1's in them.

4. Switch 'On' the power supply and press reset button.

5. Check the clock pulseof2KHzonOscilloscopeatgiventestpoint.

6. At Scientech 2121 A Block Code Encode run it now select the data at seven Segment display with the help of BCD (binary coded decimal) switch.

7. Check the data at seven segment display and its binary equivalent (d3, d2, d1, d0),in the Code Word Generator block T where bit pattern is selected in the form of 8, 4, 2, 1 format.

8. Now set the H matrix are per the condition given instep 3. In Observation Table 3.1, some example sets are given (Set 1,Set2, Set3andSet4). You can set your own

matrix or you can choose any set from example sets and select the H Matrix.

6. After that check the H matrix in the form of H= [Ik][P];Identity matrix and Parity matrix corresponding to the selected set as given in the Observation Table 3.1.

7. Check the massage signal in the form of(d3, d2, d1, d0, p3, p2, p1) and verify the status of‟ Parity Bits'(p3, p2, p1) as per the equations given for parity generation(see observation Table 3.1).

8. Connect 2mmpatchcordsbetweenhorizontalbit stream and p/s block as per the connections diagram.

9. ObservethebitpatternoutputofcodewordGeneratoratvertical7-bitstream.

10. Now connect the DataoutputtotheDataInof2121Bwhichisblockcodedecoder.

11. Now connect the clockandgroundof2121Ato 2121B via a2mmpatch cord.

12. Now set the H-Matrix section of 2121B Block code Decoder unit as per the same set what you have chose for 2121A Encoder unit. Refer the Observation Table 3.1.

13. Now first set Data '0' at Encoder unit and press reset switch until you get same decoded data on LED display and as well as at the seven segment display in numeric form. Once you get the same data 0 at decoder unit you can vary BCD switch to get the sequential data from 0-9.

14. For any selected data from 0-9, check the H matrix in the form of H=[P][Ik]; Parity matrix and Identity matrix as given in the Observation Table 3.1

15. Also check the massage signal in vertical matrix 'R' in the form of (d3, d2, d1, d0, p3, p2, p1) and check the status of SyndromeEm. As there is no error in the bits it will show (0 0 0).

16. Check the corrected code word and match it with the code word of Encoder unit.

17. Also check the Decode Bits (d3, d2, d1, d0) and match with the data at Encoder unit.

Equations for Parity Generation:

$p1 = d0 \oplus d2 \oplus d3$

$p2 = d0 \oplus d2 \oplus d3$

$p2 = d0 \oplus d1 \oplus d2$

Code Word Generator:

Identity Matrix				Parity Matrix		

Observation Table:

Decimal	Binary
7 Segment	d3 d2 d1 d0
0	
1	
2	
3	
4	
5	
6	
7	
8	
9	

Code Word
d3 d2 d1 d0 p3 p2 p1

RESULT: Linear Block Code encoding and decoding are verified.

10. Eye Diagrams, Noise and Bit Error Rate

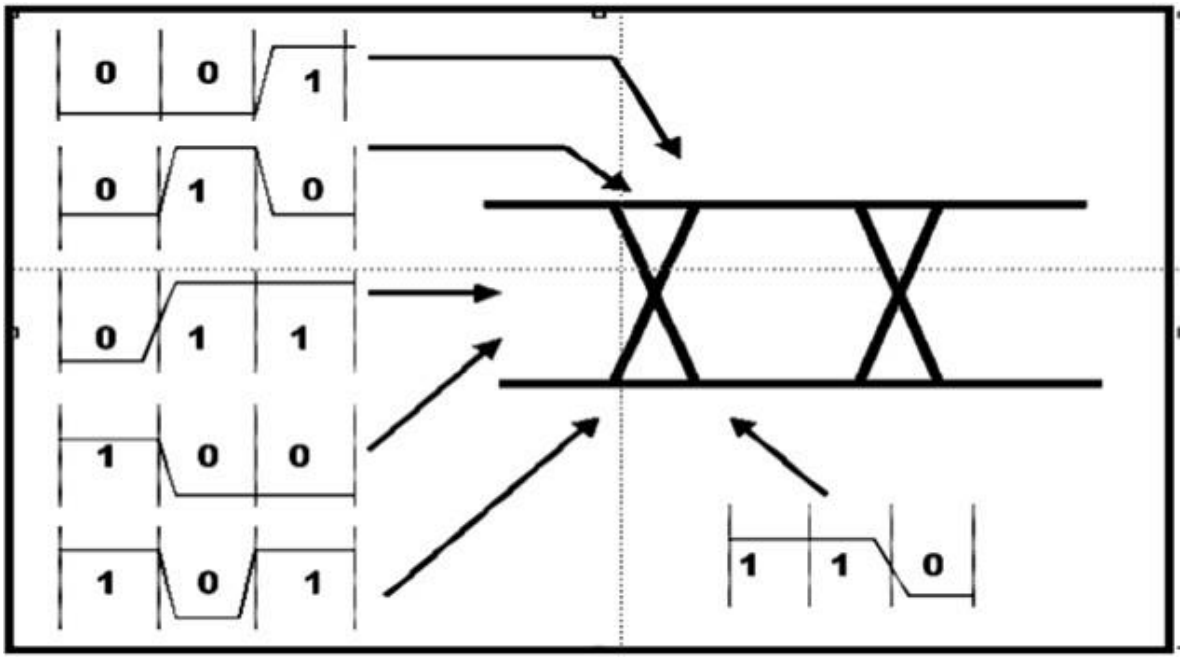
Aim: The aim of Experiment is to analyze the receiver performance by using the eye Diagrams, noise and bit error rate.

Apparatus:

- Oscilloscope
- Optical Fiber Communication Experiment Kit
- Signal generator
- Pulse Counter
- AVO meter
- Wires
- Opticalfiber:3mmulti-mode

Theory:

In telecommunication, an eye pattern, also known as an eye diagram, is an oscilloscope display in which a digital signal from a receiver is repetitively sampled and applied to the vertical input (y-axis), while the data rate is used to trigger the horizontal sweep (x-axis).

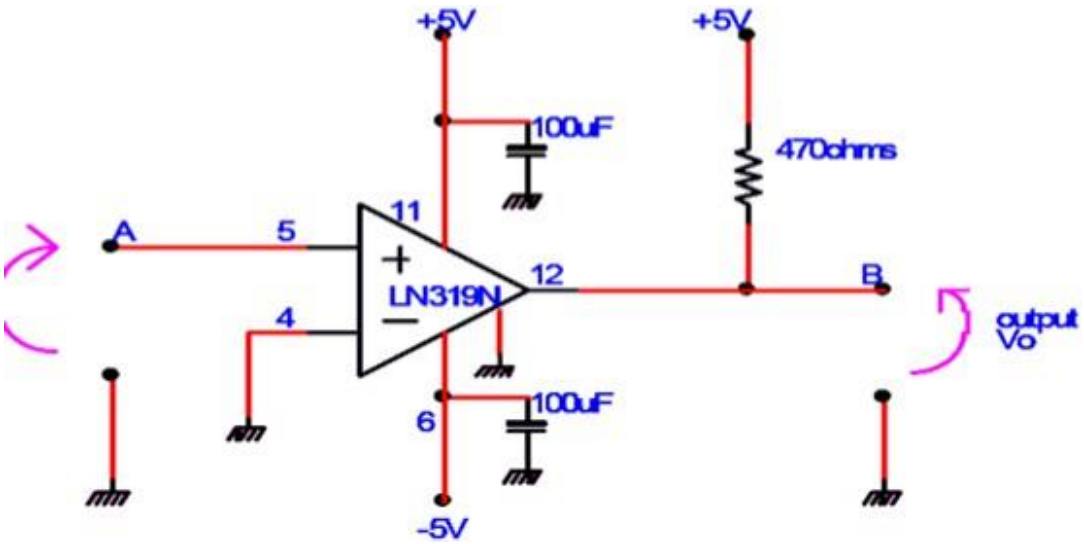


Procedure

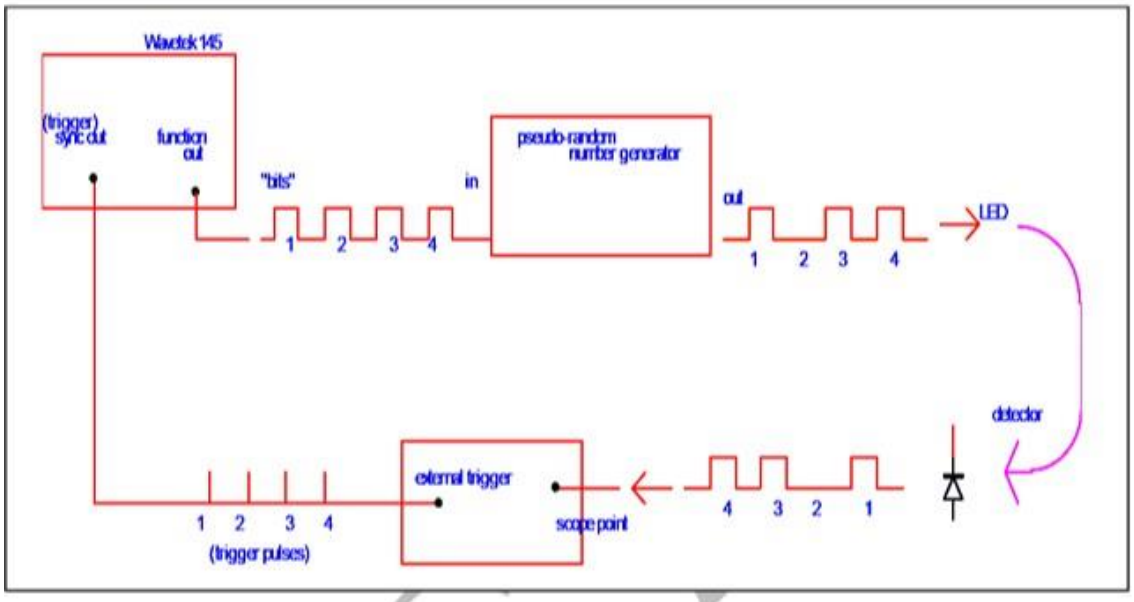
We now make an addition to the receiver, which converts the distorted detected pulses into digital logic signals again. For this, we will be using a LM311comparator with ground as our decision level.

1. Connect the output of the trans-impedance amplifier to the input of the comparator. Then by using the DC offset of the op-amp, position the amplifier waveform about the decision level (halfway between the high and low voltages) so that the comparator can make its decision. The comparator circuit is shown in Fig.

2. Connect one scope input to point A and the other to point B, and both scope inputs should be on DC since we are interested in some absolute DC threshold.



3. Set the signal generator for a100kHz, 0Vto +3Vsquarewave. Connect a coax cable from the Sync-Out on the frequency generator to the external trigger on the oscilloscope for all future triggering. When the diode is driven by the random output, the detected waveform should be your eye diagram.



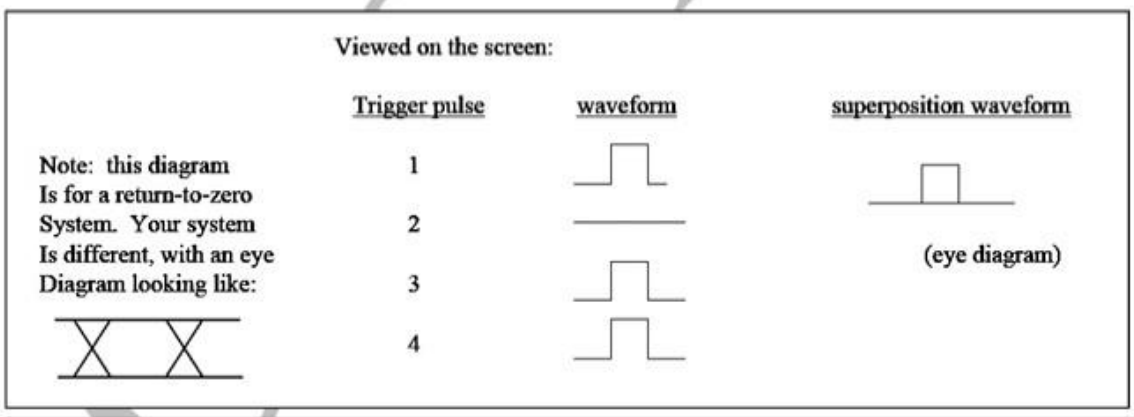


Fig.(4) shows the circuit for generating eye diagrams using a 4-bit pseudo-random number generator.

Result: