DRONACHARYA
Group of Institutions

DIGITAL SYSTEM DESIGN

LABORATORY MANUAL

BTech Semester -III

Subject Code:BEC 352

Session: 2024-25, Odd Semester

Name:	
Roll. No.:	
Group/Branch:	

DRONACHARYA GROUP OF INSTITUTIONS
DEPARTMENT OF ECE
#27 KNOWLEDGE PARK 3

GREATER NOIDA

AFFILATED TO Dr. ABDUL KALAM TECHNICAL UNIVERSITY, LUCKNOW

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Vision and Mission of the Institute

Vision:

Instilling core human values and facilitating competence to address global challenges by providing Quality Technical Education.

Mission:

- **M1 -** Enhancing technical expertise through innovative research and education, fostering creativity and excellence in problem-solving.
- **M2 -** Cultivating a culture of ethical innovation and user-focused design, ensuring technological progress enhances the well-being of society.

M3 - Equipping individuals with the technical skills and ethical values to lead and innovate responsibly in an ever-evolving digital landscape.

Vision and Mission of the Department

Vision:

To achieve excellence in Electronics and Computer engineering through quality education, research contributing to the emerging technologies and innovation to serve industry and society.

Mission:

- **M1:** To help students achieve their goals by recognizing, identifying, and to bring up their unique strengths through quality education and cutting-edge research training.
- **M2:** To facilitate adequate exposure to the students through training in the state of-the art technologies.
- **M3:** To imbibe ability in the students to solve real life problems as per need of the society through nurturing their skills, creative thinking, and research acumen.

Programme Educational Objectives (PEOs)

PEO 1.

To develop a strong foundation of engineering fundamentals to build successful careers maintaining high ethical standards.

PEO 2.

To prepare graduates for higher studies and research activities, facilitating a commitment to lifelong learning.

PEO 3.

To prepare graduates for higher studies and research activities, facilitating a commitment to lifelong learning.

Programme Outcomes (POs)

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

PSO1:

To analyses electronics systems applying principles of mathematics and engineering sciences, to develop innovative ethical solutions to complex engineering problems with team spirit and social commitment.

PSO2:

To develop solution for real world problems based on principles of computer hardware, advanced software and simulation tools with a focus to devise indigenous, eco-friendly and energy efficient projects.

University Syllabus

BEC352	**DIGITAL SYSTEM DESIGN LAB**	**0L:0T:2P**	**1 Credits**

SUGGESTIVE LIST OF EXPERIMENTS

1. Introduction to digital electronics lab- nomenclature of digital ICs, specifications, study of the data sheet, Concept of Vcc and ground, verification of the truth tables of logic gates using TTL ICs.
2. Implementation of the given Boolean function using logic gates in both SOP and POS forms.
3. Verification of state tables of RS, JK, T and D flip-flops using NAND & NOR gates.
4. Implementation and verification of Decoder using logic gates.
5. Implementation and verification of Encoder using logic gates.
6. Implementation of 4:1 multiplexer using logic gates.
7. Implementation of 1:4 demultiplexer using logic gates.
8. Implementation of 4-bit parallel adder using 7483 IC.
9. Design, and verify the 4-bit synchronous counter.
10. Design, and verify the 4-bit asynchronous counter.
11. Implementation of Mini Project using digital integrated circuits and other components.

Course outcomes:

At the end of this course students will demonstrate the ability to:

1. Design and analyze combinational logic circuits.
2. Design & analyze modular combinational circuits with MUX/DEMUX, decoder, encoder.
3. Design & analyze synchronous sequential logic circuits.
4. Design & build mini project using digital ICs.

Course Outcomes (COs)

Upon successful completion of the course, the students will be able to:

CO1	Design and analyze combinational logic circuits.
CO2	Design and analyze modular Combinational circuits with MUX / DEMUX, encoder, decoder.
CO3	Design and analyze synchronous sequential logic circuits.
CO4	Design and build mini-projects using digital ICs.

CO-PO Mapping

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3							2		1	1	2
CO2	2	3	3	3	3					1	1	2
CO3	2	3	2	2	2			1	1	1	2	1
CO4	2	3	2	2	2			1	1	1		2
Course Correlation mapping	**1.8**	**1.8**	**1.4**	**1.4**	**1.4**			**1.4**	**1**	**1.6**	**1.4**	**1.6**

Correlation Levels: High-3, Medium-2, Low-1

CO-PSO Mapping

	PSO1	**PSO2**	**PSO3**
CO1	3		2
CO2	3	3	
CO3	2	3	
CO4	1	3	
CO5	2		3
	2.2	**1.8**	**1**

Course Overview

Digital system design is a field of electronics involving the study of digital signals and the engineering of devices that use or produce them. The main components of digital electronics are diodes, transistor, logic gates and batteries. Digital electronics, digital circuits, and digital technology are electronics that are operated on digital signals. Digital techniques are much easier for getting the electronic device. These devices are used to switch into one of the known states apart from reproducing a continuous range of values. Digital circuits are made from a large collection of logic gates and a simple electronic representation of the Boolean logic function.

This manual is intended for the second year students of Electrical and Electronics engineering branch. This manual typically contains practical/Lab Sessions related Digital Electronics covering various aspects related to the subject to enhance understanding. Students are advised to thoroughly go through this manual rather than only topics mentioned in the syllabus as practical aspects are the key to understanding and conceptual visualization of theoretical aspects covered in the books.

List of Experiments mapped with COs

S. No.	Name of the Experiment	Course Outcome
1	Introduction to digital electronics lab- nomenclature of digital ICs, specifications, study of the datasheet, Concept of Vcc and ground, verification of the truth tables of logic gates using TTL ICs.	CO1
2	Implementation of the given Boolean function using logic gates in both SOP and POS forms.	CO1
3	Verification of state tables of RS, JK, T and D flip-flops using NAND & NOR gates.	CO2
4	Implementation and verification of Decoder using logic gates.	CO4
5	Implementation and verification of Encoder using logic gates.	CO4
6	Implementation of 4:1 multiplexer using logic gates.	CO3
7	Implementation of 1:4 demultiplexer using logic gates.	CO3
8	Implementation of 4-bit parallel adder using 7483 IC.	CO2
9	Design, and verify the 4-bit synchronous counter.	CO4
10	Design, and verify the 4-bit asynchronous counter.	CO4
11	Implementation of Mini Project using digital integrated circuits and other components.	CO4

DOs and DON'Ts

DOs

1. Come fully prepared for the experiment in the laboratory.
2. Check for appropriate power supply before connecting to the equipment.
3. Decide the appropriate range of the measuring instruments on the basis of quantity to be measured.
4. Make the connections without connecting the leads to the supply.
5. Re-check the connections and show it to the teacher /instructor before switching-on the power supply to the circuit.
6. Energize the circuit only with the permission of the teacher/instructor.
7. After the experiment, disconnect the connections and put back the connecting wires/leads at appropriate place.
8. Return all the apparatus to the lab-staff.
9. In case of shock, switch-off the power supply immediately.
10. Strictly follow the procedure given with the respective experiments.

DON'Ts

1. Avoid loose connections.
2. Don't touch the main power supply leads with bare hand and avoid body earth.
3. Don't use the mobile phones during laboratory.

General Safety Precautions

Precautions (In case of Injury or Electric Shock)

1. To break the victim with live electric source, use an insulator such as fire wood or plastic to break the contact. Do not touch the victim with bare hands to avoid the risk of electrifying yourself.
2. Unplug the risk of faulty equipment. If main circuit breaker is accessible, turn the circuit off.
3. If the victim is unconscious, start resuscitation immediately, use your hands to press the chest in and out to continue breathing function. Use mouth-to-mouth resuscitation if necessary.
4. Immediately call medical emergency and security. Remember! Time is critical; be best.

Precautions (In case of Fire)

1. Turn the equipment off. If power switch is not immediately accessible, take plug off.
2. If fire continues, try to curb the fire, if possible, by using the fire extinguisher or by covering it with a heavy cloth if possible isolate the burning equipment from the other surrounding equipment.
3. Sound the fire alarm by activating the nearest alarm switch located in the hallway.
4. Call security and emergency department immediately:

Emergency : 201 (Reception)

Security : 231 (Gate No.1)

Guidelines to students for report preparation

All students are required to maintain a record of the experiments conducted by them. Guidelines for its preparation are as follows: -

1) All files must contain a title page followed by an index page. ***The files will not be signed by the faculty without an entry in the index page.***

2) Student's Name, Roll number and date of conduction of experiment must be written on all pages.

3) For each experiment, the record must contain the following

(i) Aim/Objective of the experiment
(ii) Pre-experiment work (as given by the faculty)
(iii) Lab assignment questions and their solutions
(iv) Test Cases (if applicable to the course)
(v) Results/ output

Note:

1. Students must bring their lab record along with them whenever they come for the lab.

2. Students must ensure that their lab record is regularly evaluated.

Lab Assessment Criteria

An estimated 10 lab classes are conducted in a semester for each lab course. These lab classes are assessed continuously. Each lab experiment is evaluated based on 5 assessment criteria as shown in following table. Assessed performance in each experiment is used to compute Course Outcomes attainment as well as internal marks in the lab course.

Grading Criteria	Exemplary (4)	Competent (3)	Needs Improvement (2)	Poor (1)
AC1: Designing experiments	The student chooses the problems to explore.	The student chooses the problems but does not set an appropriate goal for how to explore them.	The student fails to define the problem adequately.	The student does not identify the problem.
AC2: Collecting data through observation and/or experimentation	Develops a clear procedure for investigating the problem	Observations are completed with necessary theoretical calculations and proper identification of required components.	Observations are completed with necessary theoretical calculations but without proper understanding. Obtain the correct values for only a few components after calculations. Followed the given experimental procedures but obtained results with some errors.	Observations are incomplete. Lacks the appropriate knowledge of the lab procedures.
AC3: Interpreting data	Decides what data and observations are to be collected and verified	Can decide what data and observations are to be collected but lacks the knowledge to verify	Student decides what data to gather but not sufficient	Student has no knowledge of what data and observations are to be collected
AC4: Drawing conclusions	Interprets and analyses the data in order to propose viable conclusions and solutions	Incomplete analysis of data hence the quality of conclusions drawn is not up to the mark	Cannot analyse the data or observations for any kind of conclusions.	Lacks the required knowledge to propose viable conclusions and solutions
AC5: Lab record assessment	Well-organized and confident presentation of record & ability to correlate the theoretical concepts with the concerned lab results with appropriate reasons.	Presentation of record is acceptable	Presentation of record lacks clarity and organization	No efforts were exhibited

LAB EXPERIMENTS

EXPERIMENT NO: 1

Aim: - **Introduction to Digital Electronics Lab- Nomenclature of Digital Ics, Specifications, Study of the Data Sheet, Concept of V_{cc} and Ground, Verification of the Truth Tables of Logic Gates using TTL Ics.**

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, IC's (7400, 7402, 7404, 7408, 7432, and 7486)

BRIEF THEORY:

AND Gate: The AND operation is defined as the output as (1) one if and only if all the inputs are (1) one. 7408 is the two Inputs AND gate IC.A&B are the Input terminals &Y is the Output terminal.

$$Y = A.B$$

OR Gate: The OR operation is defined as the output as (1) one if one or more than 0 inputs are (1) one. 7432 is the two Input OR gate IC. A&B are the input terminals & Y is the Output terminal.

$$Y = A + B$$

NOT GATE: The NOT gate is also known as Inverter. It has one input (A) & one output (Y). IC No. is 7404. Its logical equation is,

$$Y = A \text{ NOT } B, Y = A'$$

NAND GATE: The IC no. for NAND gate is 7400. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.

$$Y = (A. B)'$$

NOR GATE: The NOR gate has two or more input signals but only one output signal. IC 7402 is two I/P IC. The NOT- OR operation is known as NOR operation. If all the inputs are 0 then the O/P is 1. NOR gate is inverted OR gate.

$$Y = (A+B)'$$

EX-OR GATE: The EX-OR gate can have two or more inputs but produce one output. 7486 is two inputs IC. EX-OR gate is not a basic operation & can be performed using basic gates.

$$Y = A \oplus B$$

LOGIC SYMBOL:

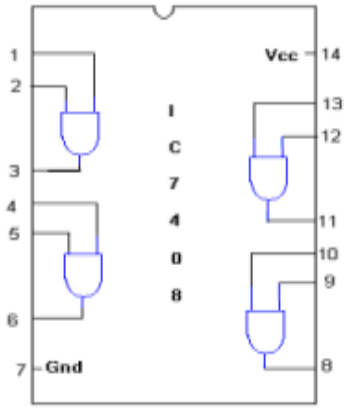
. Logic Symbol of Gates

SYMBOL:

TRUTH TABLE

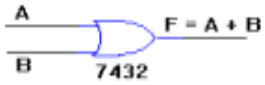
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

PIN DIAGRAM:



OR GATE:

SYMBOL:



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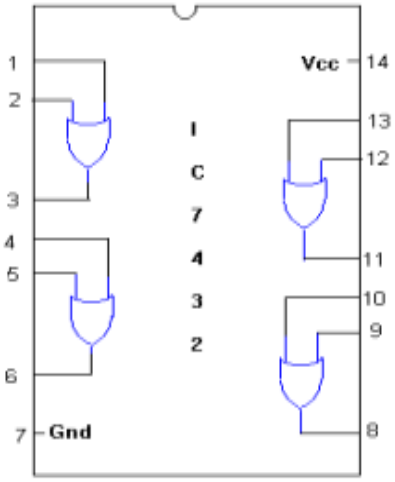


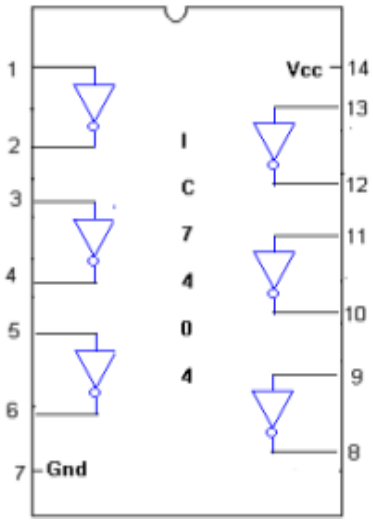
TRUTH TABLE

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE:

SYMBOL:

PIN DIAGRAM:



TRUTH TABLE :

A	$\overline{A}$
0	1
1	0

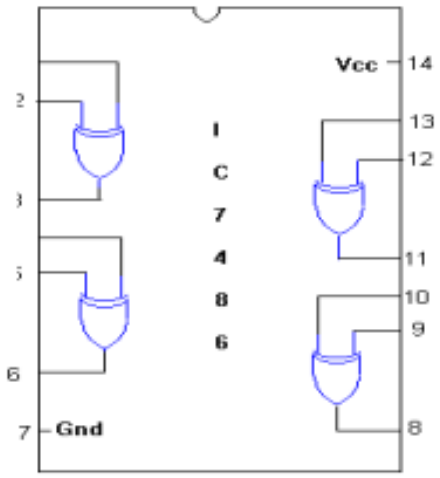
XOR GATE:

SYMBOL:

TRUTH TABLE :

A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM:



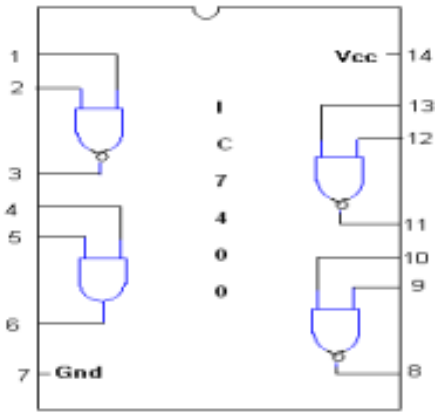
2-INPUT NAND GATE:

SYMBOL:

TRUTH TABLE

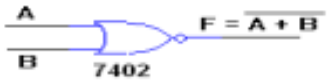
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM:



NOR GATE:

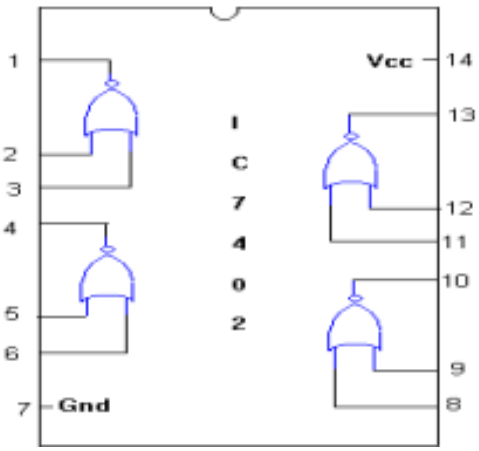
SYMBOL:



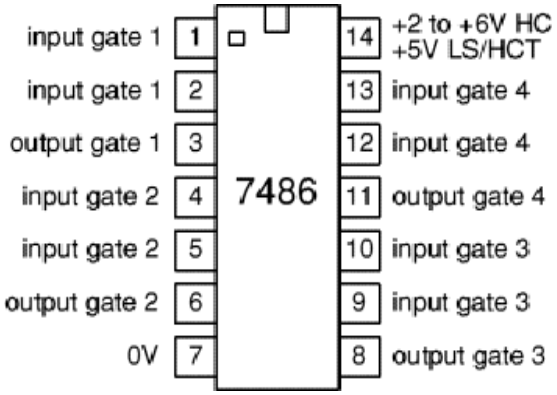
TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

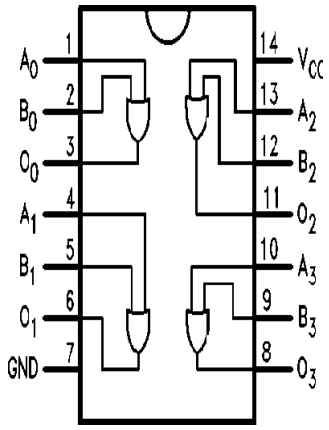
PIN DIAGRAM:



7486(EX-OR)



7432(OR)



PROCEDURE:

(a) Fix the IC's on breadboard & give the supply.
(b) Connect the +ve terminal of supply to pin 14 & -ve to pin 7.
(c) Give input at pin 1, 2 & take output from pin 3. It is same for all except NOT & NOR IC.
(d) For NOR, pin 1 is output & pin 2&3 are inputs.
(e) For NOT, pin 1 is input & pin 2 is output.
(f) Note the values of output for different combination of inputs & draw the TRUTH TABLE.

OBSERVATION TABLE:

INPUTS		**OUTPUTS**					
A	**B**	**A' NOT**	**A+B OR**	**(A+B)' NOR**	**(A*B) AND**	**(A*B)' NAND**	**(A⊕B) Ex-OR**
0	**0**	**1**	**0**	**1**	**0**	**1**	**0**
0	**1**	**1**	**1**	**0**	**0**	**1**	**1**
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**
1	**1**	**0**	**1**	**0**	**1**	**0**	**0**

RESULT: We have learnt all the gates ICs according to the IC pin diagram.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Define gates ?

Ans. Gates are the digital circuits, which perform a specific type of logical operation.

Q.2 Define IC?
Ans. IC means integrated circuit. It is the integration of no. of components on a common substrate.
Q.3 Give example of Demorgan's theorem.
Ans. (AB)'=A'+B'
(A+B)'=A'.B'
Q.4 (A+A) A =?
Ans. A.
Q5 Define Universal gates.
Ans. Universal gates are those gates by using which we can design any type of logical expression.
Q6.Write the logical equation for AND gate.
Ans. Y=A.B
Q7 How many no. of input variables can a NOT Gate have?
Ans. One.
Q8.Under what conditions the output of a two input AND gate is one?
Ans. Both the inputs are one.
Q9.1+0 =?
Ans. 1
Q10.When will the output of a NAND Gate be 0?
Ans. When all the inputs are 1.

EXPERIMENT NO: 2

Aim: Implementation of the Given Boolean Function using Logic Gates in Both SOP and POS Forms.

APPARATUS REQUIRED: Power Supply, Digital Trainer, IC's (7404, 7408, 7432) Connecting leads.

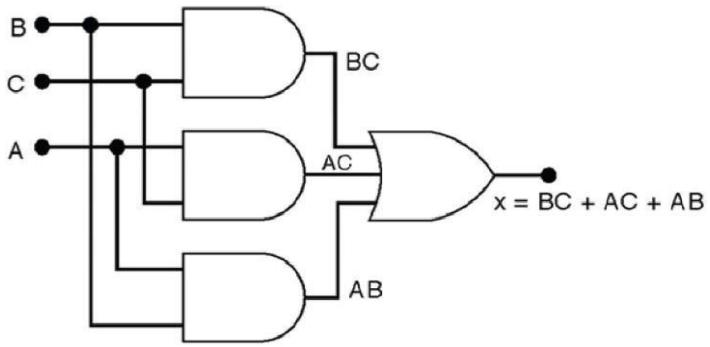
BRIEF THEORY: Karnaugh maps are the most extensively used tool for simplification of Boolean functions. It is mostly used for functions having up to six variables beyond which it becomes very cumbersome. In an n-variable K-map there are 2^n cells. Each cell corresponds to one of the combination of n variable, since there are 2^n combinations of n-variables. Gray code has been used for the identification of cells.

Example- f (A, B, C, D) =A'BC+AB'C+ABC'+ABC (SOP)

Reduced form is BC+AC+AB and POS form is f(X, Y, Z) = Y' (X'+Y+Z') (X+Z)

LOGIC DIAGRAM

SOP form



POS Form

PROCEDURE:

(a) With given equation in SOP/POS forms first of all draw a K-map.
(b) Enter the values of the O/P variable in each cell corresponding to its Min/Max term.
(c) Make group of adjacent ones.
(d) From group write the minimized equation.
(e) Design the ckt. of minimized equation & verify the truth table.

RESULT/CONCLUSION: Implementation of SOP and POS form is obtained with AND and OR gates.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Define K-map ?
Ans. It is a method of simplifying Boolean Functions in a systematic mathematical way.
Q.2 Define SOP ?
Ans. Sum of Product.
Q.3 Define POS ?
Ans. Product of Sum.
Q.4 What are combinational circuits?
Ans. These are those circuits whose output depends upon the inputs present at that instant of time.
Q.5 What are sequential circuits?
Ans. These are those circuits whose output depends upon the input present at that time as well as the previous output.
Q.6 If there are four variables how many cells the K-map will have?
Ans. 16.
Q.7 When two min-terms can be adjacent?
Ans. 2 to the power n.
Q.8 Which code is used for the identification of cells?
Ans8. Gray Code.
Q.9 Define Byte?
Ans. Byte is a combination of 8 bits.
Q.10 When simplified with Boolean Algebra $(x + y)(x + z)$ simplifies to
Ans. $x + yz$

EXPERIMENT NO: 3

Aim: Verification of State Tables of Rs, J-k, T and D Flip-Flops using NAND & NOR Gates

APPARATUS REQUIRED: IC' S 7400, 7402 Digital Trainer & Connecting leads.

BRIEF THEORY:

- **RS FLIP-FLOP:** There are two inputs to the flip-flop defined as R and S. When I/Ps R = 0 and S = 0 then O/P remains unchanged. When I/Ps R = 0 and S = 1 the flip-flop is switches to the stable state where O/P is 1 i.e. SET. The I/P condition is R = 1 and S = 0 the flip-flop is switched to the stable state where O/P is 0 i.e. RESET. The I/P condition is R = 1 and S = 1 the flip-flop is switched to the stable state where O/P is forbidden.

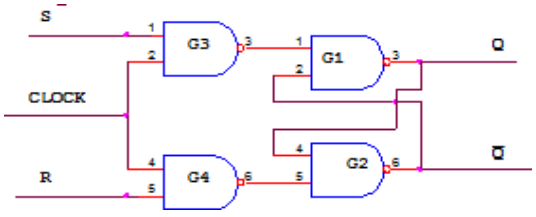
- **JK FLIP-FLOP**: For purpose of counting, the JK flip-flop is the ideal element to use. The variable J and K are called control I/Ps because they determine what the flip- flop does when a positive edge arrives. When J and K are both 0s, both AND gates are disabled and Q retains its last value.

- **D FLIP –FLOP**: This kind of flip flop prevents the value of D from reaching the Q output until clock pulses occur. When the clock is low, both AND gates are disabled D can change value without affecting the value of Q.On the other hand, when the clock is high, both AND gates are enabled. In this case, Q is forced to equal the value of D. When the clock again goes low, Q retains or stores the last value of D. a D flip flop is a bistable circuit whose Dinput is transferred to the output after a clock pulse is received.

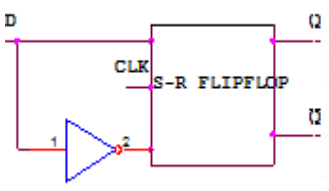
- **T FLIP-FLOP**: The T or "toggle" flip-flop changes its output on each clock edge, giving an output which is half the frequency of the signal to the T input. It is useful for constructing binary counters, frequency dividers, and general binary addition devices. It can be made from a J-K flip-flop by tying both of its inputs high.

CIRCUIT DIAGRAM:

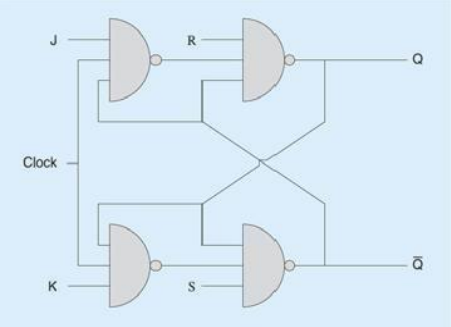
SR Flip Flop



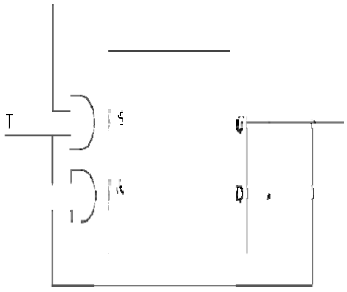
D Flip Flop



JK Flip Flop



T Flip Flop



PROCEDURE:

1. Connect the circuit as shown in figure.
2. Apply Vcc & ground signal to every IC.
3. Observe the input & output according to the truth table.

TRUTH TABLE:
SR FLIP FLOP:

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	?

D FLIPFLOP:

INPUT	OUTPUT
0	0
1	1

JK FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	0	NO CHANGE
1	0	1	0
1	1	0	1
1	1	1	Qn’

T FLIPFLOP

CLOCK	S	R	Q_{n+1}
1	0	1	NO CHANGE
1	1	0	Qn’

RESULT: Truth table is verified on digital trainer.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q 1.Flip flop is Astable or Bistable?
Ans. Bistable.
Q2.What are the I/Ps of JK flip–flop where this race round condition occurs?
Ans. Both the inputs are 1.
Q3.When RS flip-flop is said to be in a SET state?
Ans. When the output is 1.
Q4.When RS flip-flop is said to be in a RESET state?
Ans. When the output is 0.
Q5.What is the truth table of JK flip-flop?

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$Q_{n,}$

Q6.What is the function of clock signal in flip-flop?
Ans. To get the output at known time.
Q7.What is the advantage of JK flip-flop over RS flip-flop?
Ans. In RS flip-flop when both the inputs are 1 output is undetermined.
Q8.In D flip-flop I/P = 0 what is O/P?
Ans.0
Q9.In D flip-flop I/P = 1 what is O/P?
Ans.1
Q10.In T flip-flop I/P = 1 what is O/P?
Ans. Qn

EXPERIMENT NO: 4

Aim:- Implementation and Verification of Decoder/De-Multiplexer and Encoder using Logic Gates.

APPARATUS REQUIRED: IC 7447, 7-segment display, IC 74139 andconnecting leads.

BRIEF THEORY:

ENCODER: An encoder is a device, circuit, transducer, software program, algorithm or person that converts information from one format or code to another, for the purposes of standardization, speed, secrecy, security, or saving space by shrinking size. An encoder has M input and N output lines. Out of M input lines only one is activated at a time and produces equivalent code on output N lines. If a device output code has fewer bits than the input code has, the device is usually called an encoder. For example Octal-to-Binary Encoder take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1. The figure below shows the truth table of an Octal-to-binary encoder.

For an 8-to-3 binary encoder with inputs I0-I7 the logic expressions of the outputs Y0-Y2 are:

$$Y0 = I1 + I3 + I5 + I7$$

$$Y1 = I2 + I3 + I6 + I7$$

$$Y2 = I4 + I5 + I6 + I7$$

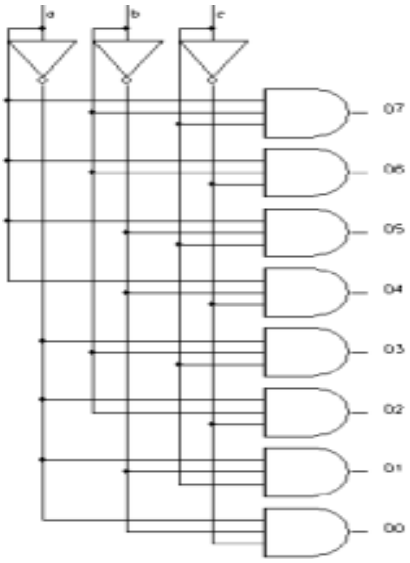
DECODER: A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight (2^3=8) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs. For any input combination decoder outputs are 1.

DEMULTIPLEXER: Demultiplexer means generally one into many. A demultiplexer is a logic circuit with one input and many outputs. By applying control signals, we can steer the input signal to one of the output lines. The ckt. has one input signal, m control

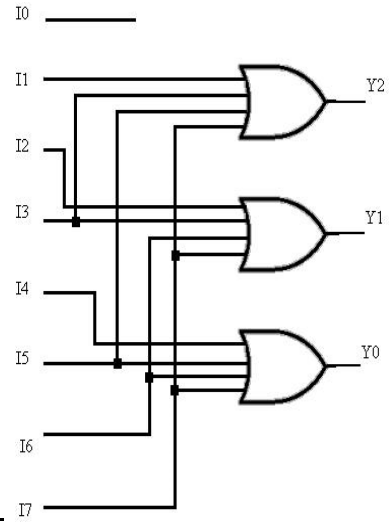
signal and n output signals. Where $2^n = m$. It functions as an electronic switch to route an incoming data signal to one of several outputs.

LOGIC DIAGRAM:

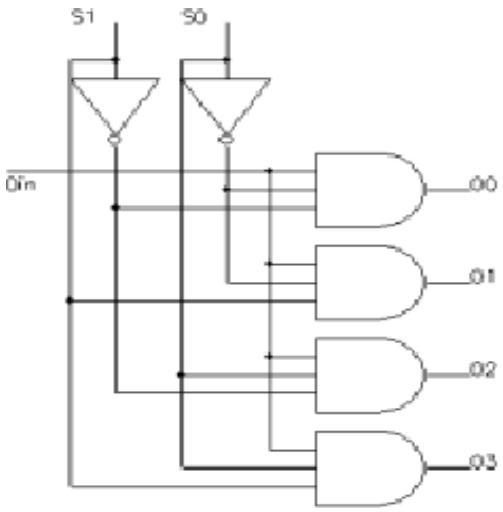
3:8 Decoder



Octal to Binary Encoder



1:4 Demux



PROCEDURE:

1) Connect the circuit as shown in figure.
2) Apply Vcc & ground signal to every IC.
3) Observe the input & output according to the truth table.

OBSERVATION TABLE:

Truth table for Decoder

Inputs			Outputs							
a	b	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1
Output function			$\bar{a}\bar{b}\bar{c}$	$\bar{a}\bar{b}c$	$\bar{a}b\bar{c}$	$\bar{a}bc$	$a\bar{b}\bar{c}$	$a\bar{b}c$	$ab\bar{c}$	abc

Truth table for Encoder

I0	I1	I2	I3	I4	I5	I6	I7	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Truth table for Demux

Output select Lines		Output selected
S_1	S_0	
0	0	O_0
0	1	O_1
1	0	O_2
1	1	O_3

RESULT: Encoder/ decoder and demultiplexer have been studied and verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q. 1 What do you understand by decoder?
Ans. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. Most IC decoders include one or more enable inputs to control the circuit operation.
Q. 2 What is demultiplexer?
Ans. The demultiplexer is the inverse of the multiplexer, in that it takes a single data input and n address inputs. It has 2^n outputs. The address input determine which data

output is going to have the same value as the data input. The other data outputs will have the value 0.

Q. 3 What do you understand by encoder?

Ans. An encoder or multiplexer is therefore a digital IC that outputs a digital code based on which of its several digital inputs is enabled.

Q. 4 What is the main difference between decoder and demultiplexer?

Ans. In decoder we have n input lines as in demultiplexer we have n select lines.

Q. 5 Why Binary is different from Gray code?

Ans. Gray code has a unique property that any two adjacent gray codes differ by only a single bit.

Q. 6 Write down the method of Binary to Gray conversion.

Ans. Using the Ex-Or gates.

Q. 7 Convert 0101 to Decimal**.**

Ans. 5

Q. 8 Write the full form of ASCII Codes?

Ans. American Standard Code for Information Interchange.

Q.9. If a register containing 0.110011 is logically added to register containing 0.101010 what would be the result?

Ans.111011

Q10.Binary code is a weighted code or not?

Ans. Yes

EXPERIMENT NO : 5

Aim: Implementation of 4x1 Multiplexer using Logic Gates.

APPARATUS REQUIRED: Power Supply, Digital Trainer, Connecting Leads, IC's 74153(4x1 multiplexer).

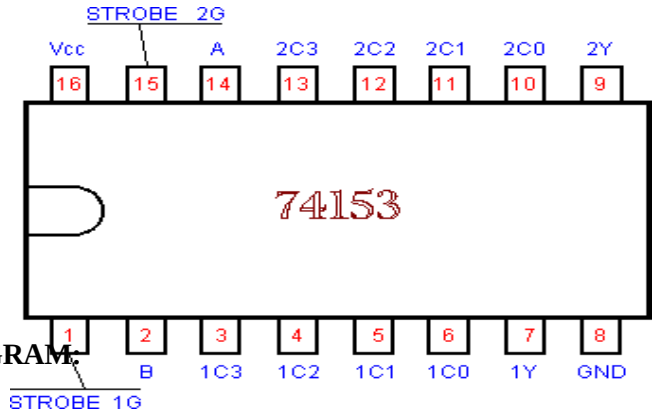
BRIEF THEORY:

MULTIPLEXER: Multiplexer generally means many into one. A multiplexer is a circuit with many Inputs but only one output. By applying control signals we can steer any input to the output .The fig. (1) Shows the general idea. The ckt. has n-input signal, control signal & one output signal. Where $2^n = m$. One of the popular multiplexer is the 16 to 1 multiplexer, which has 16 input bits, 4 control bits & 1 output bit.

PIN CONFIGURATION;–

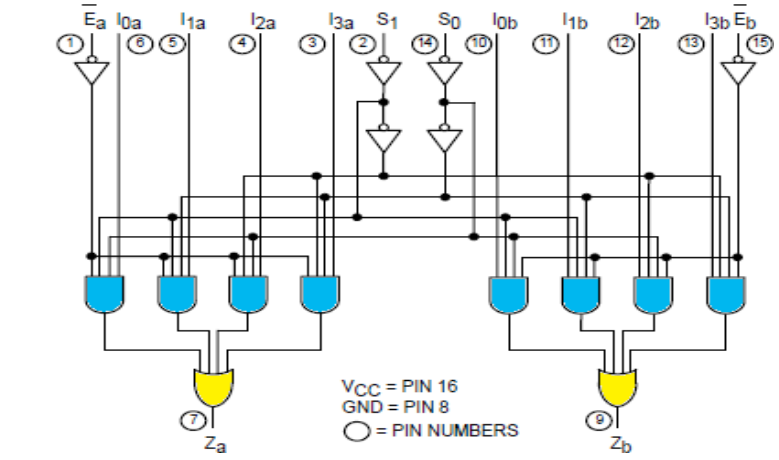
IC 74153 (4x1 multiplexer)

LOGIC DIAGRAM:



Multiplexer (4x1) IC 74153

LOGIC DIAGRAM



PROCEDURE:

1. Fix the IC's on the bread board &give the input supply.
2. Make connection according to the circuit.
3. Give select signal and strobe signal at respective pins.
4. Connect +5 v Vcc supply at pin no 24 & GND at pin no 12.
5. Verify the truth table for various inputs.

OBSERVATION TABLE:

Truth Table of multiplexer (4x1) IC 74153

INPUT							OUTPUT
A	B	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

RESULT: Verify the truth table of multiplexer for various inputs.
PRECAUTIONS:

1) Make the connections according to the IC pin diagram.

2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Why is MUX called as "Data Selector"?
Ans. This selects one out of many inputs.
Q.2 What do you mean by Multiplexing?
Ans. Multiplexing means selecting only a single input out of many inputs.
Q.3 What is Digital Multiplexer?
Ans. The multiplexer which acts on digital data.
Q.4 What is the function of Enable input to any IC?
Ans. When this enable signal is activated.
Q.5 What is demultiplexer?
Ans. A demultiplexer transmits the data from a single source to various sources.
Q.6 Can a decoder function as a D'MUX?
Ans. Yes
Q.7 What is the role of select lines in a Demultiplexer?
Ans. Select line selects the output line.
Q.8 Differentiate between functions of MUX & D'MUX?
Ans. Multiplexer has only single output but demultiplexer has many outputs.
Q.9 The number of control lines required for a 1:8 demultiplexer will be
Ans. 3
Q.10 How many 4:1 multiplexers will be required to design 8:1 multiplexer?
Ans. 2

EXPERIMENT NO - 6

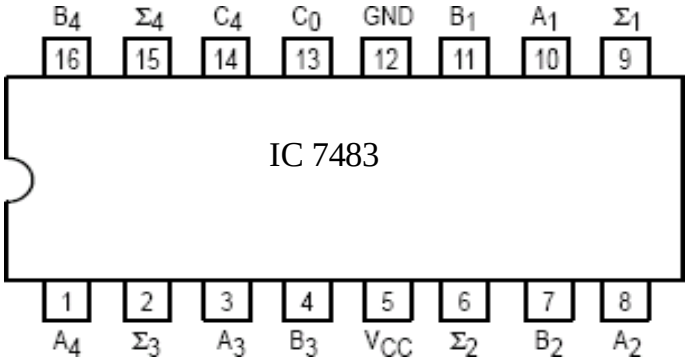
Aim – Implementation of 4-Bit Parallel Adder Using 7483 Ic.

APPRATUS REQUIRED – Digital trainer kit, IC 7483 (4-bit parallel adder).

BRIEF THEOR - A 4-bit adder is a circuit which adds two 4-bits numbers, say, A and B. In addition, a 4-bit adder will have another single-bit input which is added to the two numbers called the carry-in (C_{in}). The output of the 4-bit adder is a 4-bit sum (S) and a carry-out (C_{out}) bit.

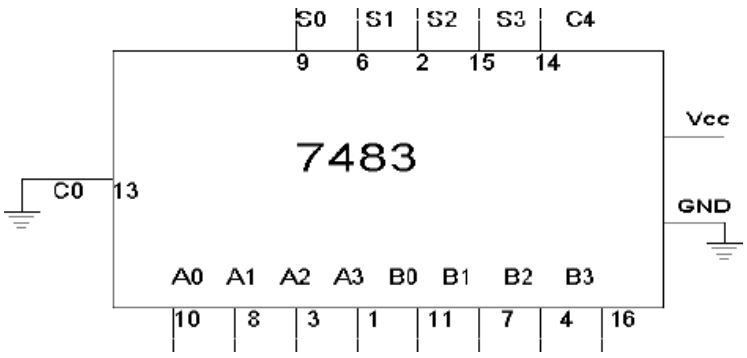
PIN CONFIGURATION–

Pin Diagram of IC 7483



LOGIC DIAGRAM:-

7483 4-bit Parallel Adder



OBSERVATION TABLE –

Truth table of 4-bit parallel adder

A3	A2	A1	A0	B3	B2	B1	B0	C4 (V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	0	1	0	0	1	0	0	0	0	1	1
0	1	0	1	1	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	0	0	1	1	0	1	0	1	0

PROCEDURE –

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT- Binary 4-bit full adder is studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q 1 What do you understand by parallel adder?
Ans. If we place full adders in parallel, we can add two- or four-digit numbers or any other size desired i.e. known as parallel adder.
Q2 What happens when an *N*-bit adder adds two numbers whose sum is greater than or equal to 2^N
Ans. Overflow.
Q3 Is Excess-3 code is weighted code or not?
Ans. Excess-3 is not a weighted code.
Q4 What is IC no. of parallel adder?
Ans. IC 7483.
Q5 What is the difference between Excess-3 & Natural BCD code?
Ans. Natural BCD code is weighted code but Excess-3 code is not weighted code.
Q6. What is the Excess-3 code for $(396)_{10}$
Ans. $(396)_{10} = (011011001001)_{EX-3}$
Q7 Can we obtain 1's complement using parallel adder?
Ans. Yes
Q8 Can we obtain 2's complement using parallel adder?
Ans. yes
Q9 How many bits can be added using IC7483 parallel adder?
Ans. 4 bits.
Q10 Can you obtain subtractor using parallel adder?
Ans. Yes

EXPERIMENT NO :7

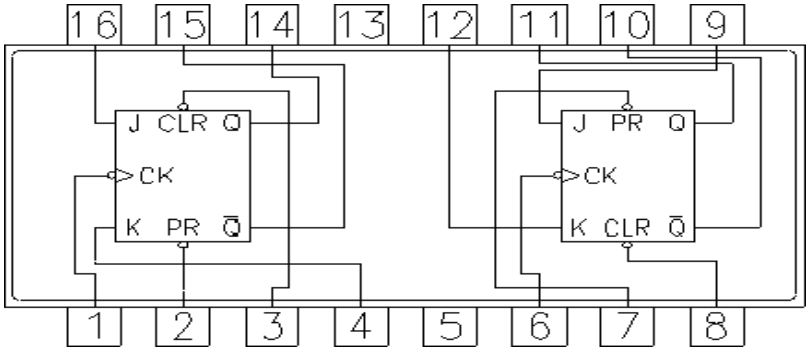
Aim: – Design, and Verify the 4-Bit Synchronous Counter

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

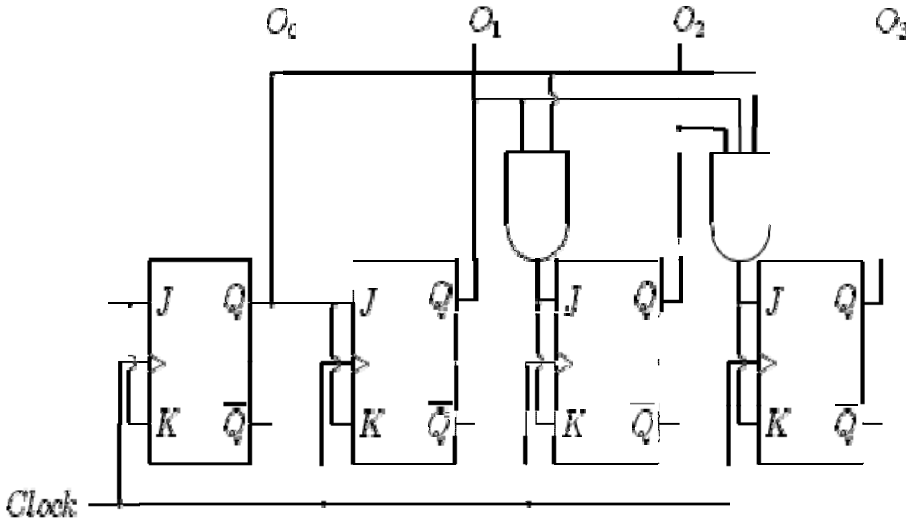
PIN CONFIGURATION:

Dual JK Master Slave Flip Flop with clear & preset



LOGIC DIAGRAM:

4-Bit Synchronous counter



Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

OBSERVATION TABLE:

Truth Table

States				**Count**
0_4	**0_3**	**0_2**	**0_1**	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6

0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT: 4-bit synchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 What do you understand by counter?
Ans. Counter is a register which counts the sequence in binary form.
Q.2What is asynchronous counter?
Ans. Clock input is applied to LSB FF. The output of first FF is connected as clock to next FF.
Q.3What is synchronous counter?
Ans. Where Clock input is common to all FF.
Q.4Which flip flop is used in asynchronous counter?
Ans. All Flip-Flops are toggling FF.
Q.5Which flip flop is used in synchronous counter?
Ans. Any FF can be used.
Q.6 What do you understand by modulus?
Ans. The total no. of states in counter is called as modulus. If counter is modulus-n, then it has n different states.
Q.7 What do you understand by state diagram?

Ans. State diagram of counter is a pictorial representation of counter states directed by arrows in graph.

Q.8 What do you understand by up/down counter?

Ans. Up/Down Synchronous Counter: two way counter which able to count up or down.

Q.9 Why Asynchronous counter is known as ripple counter?

Ans. Asynchronous Counter: flip-flop doesn't change condition simultaneously because it doesn't use single clock signal Also known as ripple counter because clock signal input as ripple through counter.

Q.10 which type of counter is used in traffic signal?

Ans. Down counters.

EXPERIMENT NO: 8

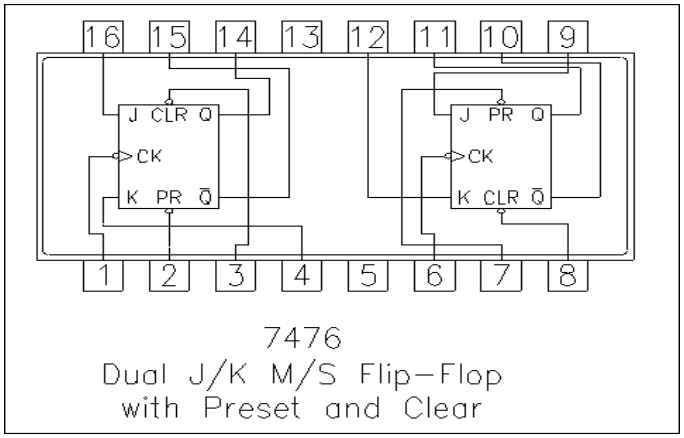
Aim: – Design, and Verify the 4-Bit Asynchronous Counter.

APPARATUS REQUIRED: Digital trainer kit and 4 JK flip flop each IC 7476 (i.e dual JK flip flop) and two AND gates IC 7408.

BRIEF THEORY: Counter is a circuit which cycle through state sequence. Two types of counter, Synchronous counter (e.g. parallel) and Asynchronous counter (e.g. ripple). In Ripple counter same flip-flop output to be used as clock signal source for other flip-flop. Synchronous counter use the same clock signal for all flip-flop.

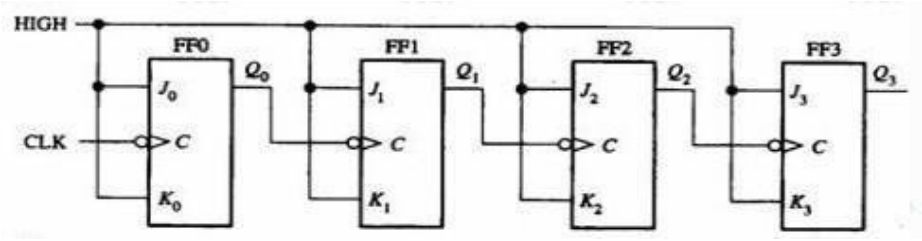
PIN CONFIGURATION:

Pin diagram of JK M/S Flip Flop



LOGIC DIAGRAM:

4-Bit Asynchronous counter



Pin Number	Description
1	Clock 1 Input
2	Preset 1 Input
3	Clear 1 Input
4	J1 Input
5	Vcc
6	Clock 2 Input
7	Preset 2 Input
8	Clear 2 Input
9	J2 Input
10	Complement Q2 Output
11	Q2 Output
12	K2 Input
13	Ground
14	Complement Q1 Output
15	Q1 Output
16	K1 Input

PROCEDURE:

a) Make the connections as per the logic diagram.
b) Connect +5v and ground according to pin configuration.
c) Apply diff combinations of inputs to the i/p terminals.
d) Note o/p for summation.
e) Verify the truth table.

RESULT: 4-bit asynchronous counter studied and verified.

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 How many flip-flops are required to make a MOD-32 binary counter?
Ans. 5.
Q.2 The terminal count of a modulus-11 binary counter is_____.
Ans.1010.
Q.3 Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:
Ans. Input clock pulses are applied simultaneously to each stage.

Q4. Synchronous construction reduces the delay time of a counter to the delay of:

Ans. a single flip-flop and a gate.

Q5. What is the difference between a 7490 and a 7492?

Ans.7490 is a MOD-10, 7492 is a MOD-12.

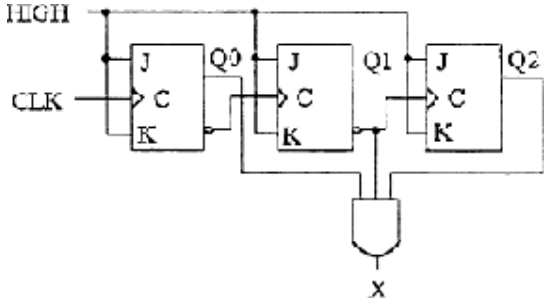
Q6. When two counters are cascaded, the overall MOD number is equal to the _____of their individual MOD numbers.

Ans. Product.

Q7. A BCD counter is a_____.

Ans. decade counter.

Q8. What decimal value is required to produce an output at "X" ?



Ans.5.

Q9. How many AND gates would be required to completely decode ALL the states of a MOD-64 counter, and how many inputs must each AND gate have?

Ans. 64 gates, 6 inputs to each gate.

Q.10 A ring counter consisting of five Flip-Flops will have

Ans. 5 states.

EXPERIMENT NO: 9

Aim:- To Design &Verify Operation of Half Adder &Full Adder.

APPARATUS REQUIRED: Power supply, IC's, Digital Trainer, Connecting leads.

BRIEF THEORY: We are familiar with ALU, which performs all arithmetic and logic operation but ALU doesn't perform/ process decimal no's. They process binary no's.

Half Adder: It is a logic circuit that adds two bits. It produces the O/P, sum & carry. The Boolean equation for sum & carry are:

$$SUM = A + B$$
$$CARRY = A.\ B$$

Therefore, sum produces 1 when A&B are different and carry is 1when A&B are 1. Application of Half adder is limited.

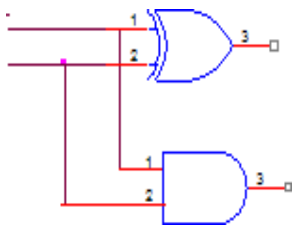
Full Adder: It is a logic circuit that can add three bits. It produces two O/P sum & carry. The Boolean Equation for sum & carry are:

$$SUM = A + B + C$$
$$CARRY = A.B + (A+B)\ C$$

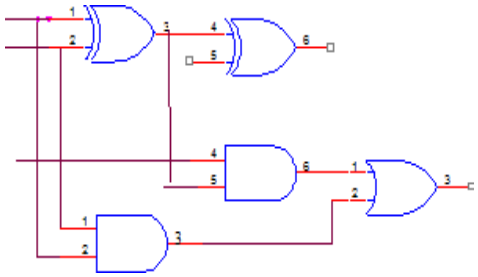
Therefore, sum produces one when I/P is containing odd no's of one & carry is one when there are two or more one in I/P.

LOGIC DAIGRAM:

Half Adder



Full Adder



PROCEDURE:

(a) Connect the ckt. as shown in fig. For half adder.
(b) Apply diff. Combination of inputs to the I/P terminal.
(c) Note O/P for Half adder.
(d) Repeat procedure for Full wave.
(e) The result should be in accordance with truth table.

OBSERVATION TABLE:

HALF ADDER:

INPUTS		OUTPUT	
A	**B**	**S**	**C**
0	**0**	**0**	**0**
0	**1**	**1**	**0**
1	**0**	**1**	**0**
1	**1**	**0**	**1**

FULL ADDER:

INPUTS			OUTPUTS	
A	**B**	**C**	**S**	**CARRY**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**1**
1	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**

RESULT: The Half Adder & Full Adder ckts. are verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q.1 Give the basic rules for binary addition?
Ans. 0+0 = 0; 0+1 = 1; 1+1 = 1 0 ; 1+0 = 1.
Q.2 Specify the no. of I/P and O/P of Half adder?
Ans2. Two inputs & one output.
Q.3 What is the drawback of half adder?
Ans. We can't add carry bit from previous stage.
Q.4 Write the equation for sum & carry of half adder?
Ans. Sum = A XOR B; carry = A.B.
Q.5 Write the equation for sum & carry of full adder?
Ans. SUM= A'B'C+A'BC'+AB'C'+ABC; CARRY=AB+BC+AC.
Q.6 How many half adders will be required for Implementing full adder?
Ans. Two half adders and a OR gate.
Q7 Define Bit?
Ans. Bit is an abbreviation for binary digit.
Q8.What is the difference b/w half adder& half sub tractor?
Ans. Half adder can add two bits & half sub tractor can subtract two bits.
Q9. Half subtractor logic circuit has one extra logic element. Name the element?
Ans. Inverter.
Q10. Define Nibble?
Ans. Combination of four bits.

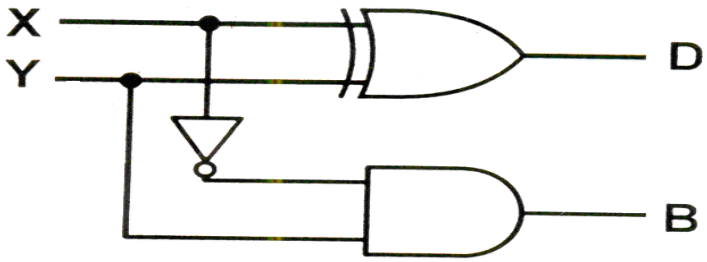
EXPERIMENT NO :10

Aim:- To Study &Verify Half Subtractor.

APPARATUS REQUIRED: Digital trainer kit,
IC 7486 (EX-OR)
IC 7408 (AND gate)
IC 7404 (NOT gate)

BRIEF THEORY: A logic circuit for the subtraction of B(subtrahend) from A (minuend) where A& B are 1 bit numbers is referred as half- sub tractor.

LOGIC DIAGRAM :



TRUTH TABLE:

INPUT 1 (X)	INPUT 2 (Y)	BORROW (B)	DIFFERENCE (D)
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

PROCEDURE:

1. Make the connections as per the logic diagram.
2. Connect +5v to pin 14 & ground to pin 7.
3. Apply 0 to input X & Y as per the truth table.
4. Switch on the instrument.
5. Observe the reading on 8 bits LED display.
6. Repeat steps 3 & 5 for different input as per truth table.
7. Verify the truth table.

RESULT: Half sub tractor circuit is studied and verified**.**

Quiz Questions with answer.

Q.1 What is half subs tractor?
Ans. Performs subs traction of two bits.
Q.2 For implementing half subs tractor how many EX-OR, AND gates and Not gates are required?
Ans. One EX-OR, one –AND gate, one- Not gate.
Q.3 What are the logical equations for difference & borrow?
Ans. $D = \bar{A}B + A\bar{B}$
$B = \bar{A}.B$
Q.4 How full subtractor is different from half subs tractor.
Ans. Full sub tractor performs subtraction of three bits but half subs tractor Performs subtraction of two bits.
Q5 If inputs of half subs tractor are A=0, and B=1 then Borrow will be?
Ans. B=1
Q.6 Is 2's complement method appropriate for subtraction?
Ans. 2's complement method is appropriate method for subtraction.
Q.7 How many bits we use in half subtractor for subtraction?
Ans. only two bits.
Q.8Can we use parallel adder for subtraction?
Ans. We can use parallel adder using 2's complement method.
Q.9 Which one is better subtractor or parallel adder for subtraction?
Ans. Parallel adder is the best option using 1's complement or 2's complement
Q.10 Which adder is used for addition of BCD numbers?
Ans. BCD adder.

EXPERIMENT NO: 11

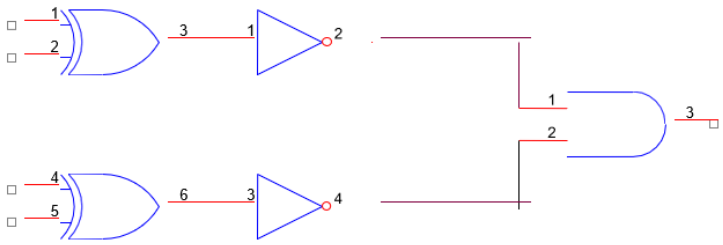
Aim: - To Design & Verify the Operation of Magnitude Comparator

APPARATUS REQUIRED: Power Supply, Digital Trainer Kit., Connecting Leads, and IC's (7404, 7408, and 7486).

BRIEF THEORY: Comparator compares the value of signal at the input. It can be designed to compare many bits. The adjoining figure shows the block diagram of comparator. Here it receives to two 2-bit numbers at the input & the comparison is at the output.

CIRCUIT DIAGRAM:

Comparator



PROCEDURE:

a. Make the connections according to the circuit diagram.
b. The output is high if both the inputs are equal.
c. Verify the truth table for different values.

OBSERVATION TABLE:

P 0	Q 0	P 1	Q 1	LOW IF P IS NOT EQUALTO Q	HIGH IF Q IS EQUAL TO Q
0	0	0	0		HIGH
1	1	0	0		HIGH
0	1	0	1	LOW	
1	0	1	0	LOW	

RESULT: The comparator is designed & verified.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer.

Q1.What is comparator?

Ans. Comparator compares the inputs (bits).

Q2. What are universal gates?
Ans. NAND, NOR.

Q3. What is the full form of BCD?
Ans. Binary Coded decimal.
Q4. What is the base of binary number system?
Ans. 2
Q5How many bits are there in one byte?
Ans. 8
Q6. How many digits are there in octal number system?
Ans. 8
Q7. What is the binary no. equivalent to decimal no. 20?
Ans. 10100
Q8. How decimal no. minus 7 can be represented by 4 bit signed binary no's?
Ans. 1111
Q9.Convert the octal no 67 into binary no.?
Ans. 110111
Q10.A binary digit is called?
Ans. Bit.

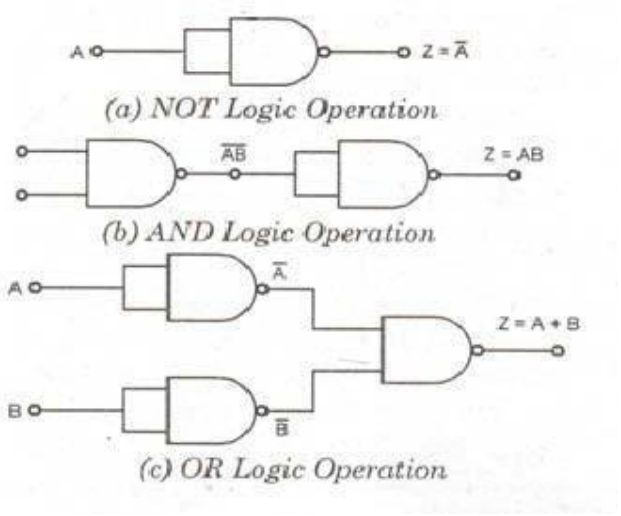
EXPERIMENT NO:12

Aim: - To Study and Verify NAND as a Universal Gate.

APPARATUS REQUIRED: Digital trainer kit, IC 7400 (NAND gate)

BRIEF THEORY: NAND OR NOR sufficient for the realization of any logic expression. because of this reason, NAND and NOR gates are known as UNIVERSAL gates.

LOGIC DIAGRAM:



TRUTH TABLE:
NAND GATE AS INVERTER: The circuit diagram of implementation of NAND gate as inverter.

A	Y
0	1
1	0

NAND GATE AS AND GATE:
The circuit diagram of implementation of NAND Gate as AND Gate.

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NAND GATE AS OR GATE:
The circuit diagram of implementation of NAND Gate as OR Gate.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

PROCEDURE:

1. Make the connections as per the logic diagram.
2. Connect +5v to pin 14 & ground to pin 7.
3. Apply diff combinations of inputs to the i/p terminals.
4. Note o/p for NAND as universal gate.
5. Verify the truth table.

Quiz Questions with answer.

Q.1 Define Gates.
Ans. Gates are digital circuit, which perform a specific type of logical operation.
Q.2 Define IC?
Ans. IC means Integrated Circuit It is the integration of no. of components on a common substrate.
Q.3 (A+A) A=?
Ans. A.
Q.4. Define universal gates
Ans. We can design any type of logical expression by using universal gates.
Q.5 Will the output of a NAND Gate be 0.
Ans. When all the inputs are1.
Q.6 Which IC is used for NAND GATE?
Ans. IC 7400.
Q.7 Why NAND is called as universal gate?
Ans. Because all gates can be made using circuits.
Q.8 Name any other universal gate?
Ans. NOR Gate.
Q.9 Which type of TTL gates can drive CMOS Gate?
Ans. TTL with open collector can derive CMOS.
Q.10 What is meant by literal?
Ans. A logical variable in a complemented or Un-complemented form is called a literal.

EXPERIMENT NO:13

AIM: - To Study 4 Bit ALU(IC 74181).

APPARATUS REQUIRED: IC 74181, etc.

BRIEF THEORY:

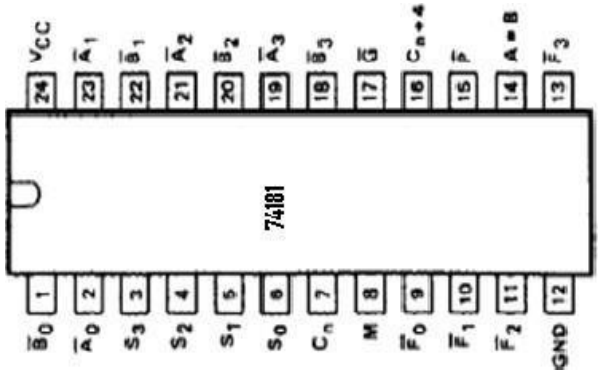
The 74181 is a 7400 series medium-scale integration (MSI) TTL integrated circuit, containing the equivalent of 75 logic gates and most commonly packaged as a 24-pin DIP. The 4-bit wide ALU can perform all the traditional add / subtract / decrement operations with or without carry, as well as AND / NAND, OR / NOR, XOR, and shift. Many variations of these basic functions are available, for a total of 16arithmetic and 16 logical operations on two four-bit words. Multiply and divide functions are not provided but can be performed in multiple steps using the shift andadd or subtract functions. Shift is not an explicit function but can be derived from several available functions including (A+B) plus A.

PIN DETAIL & FUNCTION TABLE:

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 22, 20, 18	$\overline{B}_0$ to $\overline{B}_3$	operand inputs (active LOW)
2, 23, 21, 19	$\overline{A}_0$ to $\overline{A}_3$	operand inputs (active LOW)
6, 5, 4, 3	S_0 to S_3	select inputs
7	C_n	carry input
8	M	mode control input
9, 10, 11, 13	$\overline{F}_0$ to $\overline{F}_3$	function outputs (active LOW)
12	GND	ground (0 V)
14	A=B	comparator output
15	$\overline{P}$	carry propagate output (active LOW)
16	C_{n+4}	carry output
17	$\overline{G}$	carry generate output (active LOW)
24	V_{CC}	positive supply voltage

IC 74181



FUNCTION TABLES

MODE SELECT INPUTS				ACTIVE HIGH INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC[2] (M=L; C_n=H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A + B}$	A + B
L	L	H	L	$\overline{AB}$	$A + \overline{B}$
L	L	H	H	logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$A\overline{B}$	$A\overline{B}$ minus 1
H	L	L	L	$\overline{A} + B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$(A + \overline{B})$ plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	logical 1	A plus A[1]
H	H	L	H	$A + \overline{B}$	(A + B) plus A
H	H	H	L	A + B	$(A + \overline{B})$ plus A
H	H	H	H	A	A minus 1

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M=H)	ARITHMETIC[2] (M=L; C_n=L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A} + B$	$A\overline{B}$ minus 1
L	L	H	H	logical 1	minus 1
L	H	L	L	$\overline{A + B}$	A plus $(A + \overline{B})$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$
H	L	L	L	$\overline{AB}$	A plus $(A + \overline{B})$
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)
H	L	H	H	$A + \overline{B}$	$A + \overline{B}$
H	H	L	L	logical 0	A plus A[1]
H	H	L	H	$A\overline{B}$	AB plus A
H	H	H	L	AB	$A\overline{B}$ plus A
H	H	H	H	A	A

Notes to the function tables

1. Each bit is shifted to the next more significant position.
2. Arithmetic operations expressed in 2s complement notation.

H = HIGH voltage level
L = LOW voltage level

PROCEDURE:

1. Connections are made as shown in the Circuit diagram.
2. Change the values of the inputs and verify at least 5 functions given in the function table

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The V_{cc} and ground should be applied carefully at the specified pin only.

Quiz Questions with answer

Q.1What is the difference between a mnemonic code and machine code?

Ans. Machine codes are in binary, mnemonic codes are in shorthand English.

Q.2 Which bus is a bidirectional bus?

Ans. Data Bus.

Q.3 Which of the following buses is primarily used to carry signals that direct other ICs to find out what type of operation is being performed?

Ans. control bus.

Q.4 Which of the following are the three basic sections of a microprocessor unit?

Ans. control and timing, register, and arithmetic/logic unit (ALU).
Q.5 The 8085A is a(n):
Ans. A 8-bi 8-bit parallel CPU.

Q.6 A register in the microprocessor that keeps track of the answer or results of any arithmetic or logic operation is the:

Ans. Accumulator.

Q.7 When was the first 8-bit microprocessor introduced?

Ans.1971

Q.8 What type of circuit is used at the interface point of an output port?

Ans. Latch.

Q.9 What type of circuit is used at the interface point of an input port?

Ans. Tri-state buffer.

Q.10 The register in the 8085A that is used to keep track of the memory address of the next op-code to be run in the program is the:

Ans. program counter.

EXPERIMENT NO:14

LIST OF MINI PROJECTS

1. IR Remote Switch
2. Clap Switch
3. Water-Level Controller
4. LED-Based Message Display
5. Ultra-Bright LED Lamp
6. Ding-Dong Bell Infrared Cordless Headphone
7. Mobile Phone Battery Charger
8. Telephone Number Display
9. Automatic Night Lamp With Morning Alarm
10. Three-Colour Display Using Bi-Colour LEDs
11. Remote-Operated Musical Bell
12. Simple Telephone Ring Tone Generator
13. Anti-Theft Alarm For Bikes
14. Automatic Speed-Controller For Fans and Coolers
15. Digital Stop Watch
16. Power-Supply Failure Alarm
17. Dark Room Timer
18. Remote-Controlled Power-Off Switch
19. Simple Low-Cost Digital Code Lock
20. Number Guessing Game
21. Fire Alarm Using Thermistor
22. Simple Analogue To Digital Converter
23. PC-Based 7-Segment Rolling Display
24. IR Burglar Deterrent
25. Variable Power Supply Using a Fixed-Voltage Regulator IC
26. Digital Speedometer
27. Heat-Sensitive Switch
28. Fully Automatic Emergency Light
29. Running Message Display
30. School/College Quiz Buzzer
31. Digital Dice With Numeric Display
32. Dancing Lights
33. Ready -To-Use Object Counter Laptop Protector
34. PC Based Digital Clock
35. Fancy Christmas Light

AN EXAMPLE

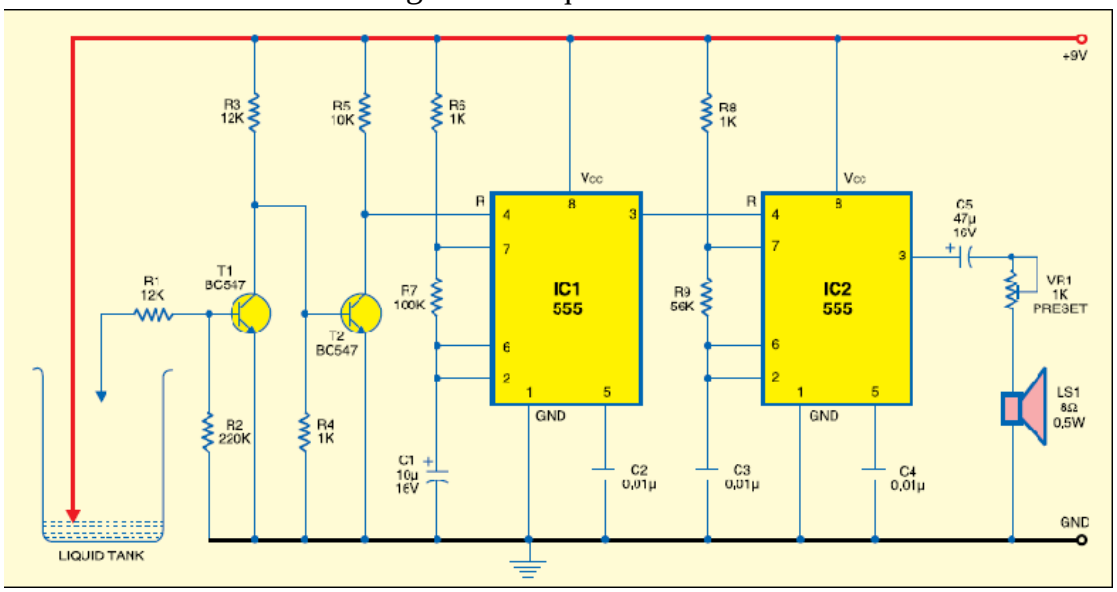
AIM: - Liquid Level Alarm

APPARATUS REQUIRED: Components as shown in the circuit diagram (such as 555IC,, soldering iron and solder flux and PCB board .

BRIEF THEORY: Here is a simple circuit for (T1 and T2) and two timers 555 ICs (IC1 and IC2). Both IC1 and IC2 are wired in astable multivibrator mode. Timer IC1 produces low frequency, while timer IC2 produces high frequency. As a result, a beeping tone is generated when the liquid tank is full. Initially, when the tank is empty, transistor T1 does not conduct. Consequently, transistor T2 conducts and pin 4of IC1 is low. This low voltage disables IC1 and it does not oscillate. The low outputof IC1 disables IC2 and it does not oscillate. As a result, no sound is heard from the speaker. But when the tank gets filled up, transistor T1 conducts. Consequently, transistor T2 is cut off and pin 4 of IC1 becomes high. This high voltage enables IC1and it oscillates to produce low frequencies at pin 3. This low-frequency output enables IC2 and it also oscillates to produce high frequencies. As a result, sound is produced from the speaker. Using preset VR1 you can control the volume of the sound from the speaker. The circuit can be powered from a 9V battery or from mainsby using a 9V power adaptor.

CIRCUIT DIAGRAM:

Cirrcuit Diagram of Liquid Level Alarm



PROCEDURE: Assemble the circuit on a general purpose PCB and enclose in a suitable cabinet. Install two water-level probes using metal strips such that one touches the bottom of the tank and the other touches the maximum level of the waterin the tank. Interconnect the sensor and the circuit using a flexible wire.

PRECAUTIONS:

1) Make the connections according to the Circuit diagram using soldering iron
2) The connections should be tight.

The V_{cc} and ground should be applied carefully at the specified pi

This lab manual has been updated by

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Crosschecked By
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Please spare some time to provide your valuable feedback.