DRONACHARYA
Group of Institutions

VLSI DESIGN LAB

LABORATORY MANUAL

B.Tech. Semester –VIITH

Subject Code: KEC 751 B/ KECZ 751 A

Session: 2024-25, Odd Semester

Name:	
Roll.No.:	
Group/Branch:	

DRONACHARYA GROUP OF INSTITUTIONS

DEPARTMENT OF ECE

#27KNOWLEDGEPARK3 GREATER NOIDA

AFFILATED TO Dr. ABDUL KALAM TECHNICALUNIVERSITY, LUCKNOW

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Vision and Mission of the Institute

Vision:

Instilling core human values and facilitating competence to address global challenges by providing Quality Technical Education.

Mission:

M1 - Enhancing technical expertise through innovative research and education, fostering creativity and excellence in problem-solving.

M2 - Cultivating a culture of ethical innovation and user-focused design, ensuring technological progress enhances the well-being of society.

M3 - Equipping individuals with the technical skills and ethical values to lead and innovate responsibly in an ever-evolving digital landscape.

Vision and Mission of the Department

VISION

To achieve excellence in Electronics and Computer engineering through quality education, research contributing to the emerging technologies and innovation to serve industry and society.

MISSION

- **M1:** To help students achieve their goals by recognizing, identifying, and to bring up their unique strengths through quality education and cutting-edge research training.
- **M2:** To facilitate adequate exposure to the students through training in the state of-the art technologies.
- **M3:** To imbibe ability in the students to solve real life problems as per need of the society through nurturing their skills, creative thinking, and research acumen.

Programme Educational Objectives (PEOs)

- **PEO1:** To develop a strong foundation of engineering fundamentals to build successful careers maintaining high ethical standards.
- **PEO2:** To prepare graduates for higher studies and research activities, facilitating a commitment to lifelong learning.
- **PEO3:** Impart strong profession, ethical, social responsibility, integrity with environmental sensitivity.

Programme Outcomes (POs)

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

- **PSO1:** To analyses electronics systems applying principles of mathematics and engineering sciences, to develop innovative ethical solutions to complex engineering problems with team spirit and social commitment.
- **PSO2:** To develop solution for real world problems based on principles of computer hardware, advanced software and simulation tools with a focus to devise indigenous, eco-friendly and energy efficient projects.

University Syllabus

KEC-751 B/ KECZ 751 A	VLSI DESIGN Lab	0L:0T:2P	1 Credit

SUGGESTIVE LIST OF EXPERIMENTS

S.No	Title	Date	Remarks
1	Design and analysis of basic of logic Gates: AND, OR, NOT, NAND, NOR, XOR, XNOR using CMOS logic.		
2	Design and implementation of Half adder and Full adder using CMOS logic.		
3	To simulate the schematic of the common drain amplifier.		
4	To simulate the schematic of the differential amplifier.		
5	To simulate the schematic of the 2-Stage Operational Amplifier.		
6	Design of 2-4 decoder using MOS technology.		
7	Design of 4:1 mux using transmission gate.		
8	Design and implementation of Flip flop circuit.		
9	Layout design CMOS inverters and its analysis		

Course Outcomes (COs)

Upon successful completion of the course, the students will be able to:

CO1	Designing of logic gates.
CO2	Implementation of combinational and sequential circuits using CMOS logic.
CO3	Analyze amplifier circuits.
CO4	Design sequential circuits such as flip flop
CO5	Do the layout designing for physical analysis of the MOS transistor and MOS based circuits.

CO-PO Mapping

	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**
CO1	3	-	-	-	1	-	-	-	1	2	-	2
CO2	3	2	-	-	2	-	-	-	1	2	-	2
CO3	2	2	2	2	-	-	-	-	1	1	-	1
CO4	2	-	2	2	2	-	-	-	1	1	-	1
CO5	2	-	2	2	2	-	-	-	1	1	-	1
Course Correlation mapping	**2.2**	**1.2**	**1.4**	**1.2**	**1.4**	**-**	**-**	**-**	**1**	**1.4**	**-**	**1.6**

Correlation Levels: High-3, Medium-2, Low-1

CO-PSO Mapping

	PSO1	PSO2	PSO3
CO1	2	3	1
CO2	2	3	1
CO3	2	3	1
CO4	2	3	1
CO5	2	3	1
	2	3	1

Course Overview

The significance of the VLSI Design Lab is renowned in the various fields of engineering applications. For an Electrical Engineer, it is obligatory to have the practical ideas about the VLSI Design. By this perspective we have introduced a Laboratory manual cum Observation for VLSI Design. The manual uses the plan, cogent and simple language to explain the fundamental aspects of VLSI Design in practical. The manual prepared very carefully with our level best. It gives all the steps in executing an experiment.

Dos and DON'Ts

DOs

1. Login-on with your user name and password.
2. Log off the computer every time when you leave the Lab.
3. Arrange your chair properly when you are leaving the lab.
4. Put your bags in the designated area.
5. Ask permission to print.

DON'Ts

1. Do not share your user name and password.
2. Do not remove or disconnect cables or hardware parts.
3. Do not personalize the computer setting.
4. Do not run programs that continue to execute after you logoff.
5. Do not down load or install any programs, games or music on computer in Lab.
6. Personal Internet use chat room for Instant Messaging (IM) and Sites is strictly prohibited.
7. No Internet gaming activities are allowed.
8. Tea, Coffee, Water & Eatables are not allowed in the Computer Lab.

Guide lines to students for report preparation

All students are required to maintain a record of the experiments conducted by them. Guidelines for its preparation are as follows: -

1) All files must contain a title page followed by an index page. The files will not be signed by the faculty without an entry in the index page.

2) Student's Name, Roll number and date of conduction of experiment must be written on all pages.

3) For each experiment, the record must contain the following

(i) Aim/Objective of the experiment
(ii) Pre-experiment work (as given by the faculty)
(iii) Lab assignment questions and their solutions
(iv) Test Cases (if applicable to the course)
(v) Results/output

Note:

1. Studentsmustbringtheirlabrecordalongwiththemwhenevertheycomeforthelab.

2. Students must ensure that their lab record is regularly evaluated.

Lab Assessment Criteria

An estimated 10 lab classes are conducted in a semester for each lab course. These lab classes are assessed continuously. Each lab experiment is evaluated based on 5 assessment criteria as shown in following table. Assessed performance in each experiment is used to compute CO attainment as well as internal marks in the lab course.

Grading Criteria	Exemplary(4)	Competent(3)	Needs Improvement(2)	Poor(1)
AC1: Designing experiments	The student chooses the Problems to explore.	The student chooses the Problems but does not set an appropriate goal For how to explore them.	The student fails to Define the problem adequately.	The student does not Identify the problem.
AC2: Collecting data through observation and/or experimentation	Develops a clear Procedure for Investigating the Problem	Observations are Completed with Necessary theoretical Calculations and proper Identification of required components.	Observations are Completed with Necessary theoretical Calculations but without Proper understanding. Obtain the correct Values for only a few Components after Calculations. Followed The given experimental Procedures but obtained Results with some errors.	Observations are In complete. Lacks the Appropriate knowledge Of the lab procedures.
AC3: Interpreting data	Decides what data and Observations are to be collected and verified	Can decide what data and observations are to be collected but lacks the Knowledge to verify	Student decides what Data to gather but not sufficient	Student has no Knowledge of what data and observations are to be collected
AC4: Drawing conclusions	Interprets and analyses The data in order to propose viable Conclusions and solutions	Incomplete analysis of Data hence the quality of conclusions drawn is not upto the mark.	Cannot analyze the data or observations for any kind of conclusions.	Lacks the required knowledge to propose viable conclusions and solutions
AC5: Lab record assessment	Well-organized and Confident presentation of record & ability to correlate the theoretical Concepts with the Concerned lab results With appropriate reasons.	Presentation of record is acceptable	Presentation of record Lacks clarity and organization	No efforts were exhibited

LAB EXPERIMENTS

Experiment 1

Aim: Design and analysis of basic of logic Gates: AND, OR, NOT, NAND, NOR, XOR, XNOR using CMOC logic.

Tool Used: e-Simand LTspice Simulator

Theory:

Static logic is a design methodology in integrated circuit design where there is at all times some mechanism to drive the output either high or low. For example, in many of the popular logic families, such as TTL and traditional CMOS, there is always a low-impedance path between the output and either the supply voltage or the ground. The most widely used logic style is static CMOS. A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0 (based on the inputs). The PUN and PDN networks are constructed in a mutually exclusive fashion such that, one and only one of these networks is conducting in the steady state.

Dynamic logic is a design methodology in integrated circuit design in that it uses a clock signal in its implementation of combinational logic circuits. In dynamic logic, there is not always a mechanism driving the output high or low. In the most common version of this concept, the output is driven high or low during distinct parts of the clock cycle. Dynamic logic requires a minimum clock rate fast enough that the output state of each dynamic gate is used before it leaks out of the capacitance holding that state.

Figure 1: all logic gates and their Truth Table

Figure 2: CMOS logic diagram of logic gates

Figure 3: CMOS logic diagram of two input XOR gate

Figure 4: CMOS logic diagram of two input XNOR gate

Procedure:

1. Download LT spice and e simfrom Internet and install it . as per given instructions .
2. Open LTspice for Circuit design.

Figure 4 window open in Lt spice

3. Open Circuit designing window .

Figure 5 Command window open in Lt spice

Circuit Diagram: AND gate:

Figure 6Circuit diagram AND gate using CMOS logic:

Result : AND gate

Figure 7 Output waveform of AND gate in simulator

OR gate:

Figure 8 Circuit diagram OR gate using CMOS logic:

Result of OR gate

Figure 9 Output waveform of OR gate in simulator

NAND gate circuit diagram

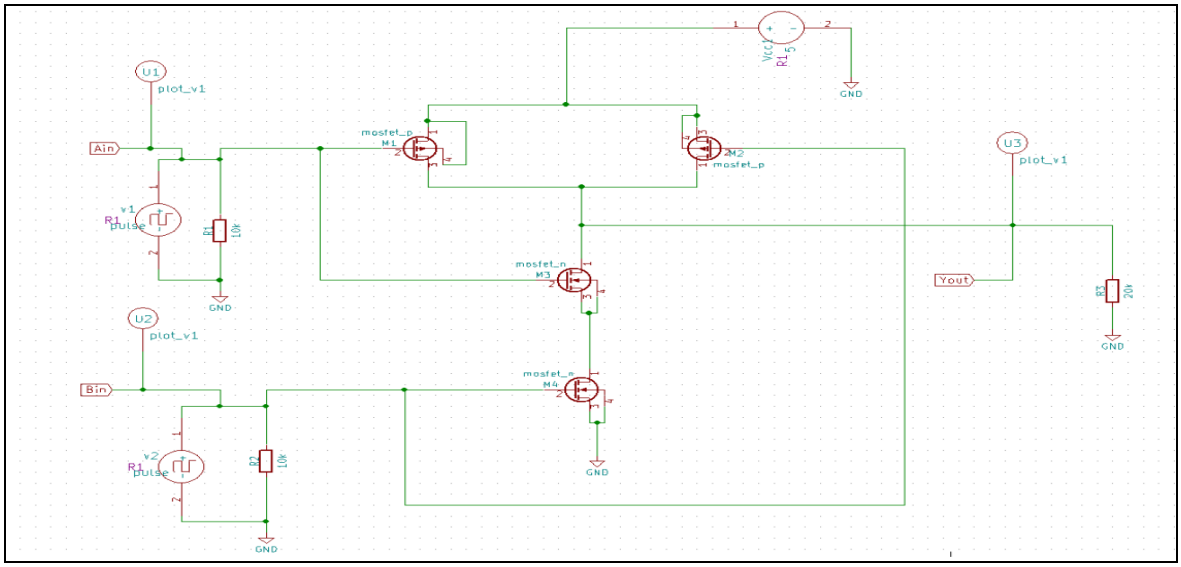


Figure 10 Circuit diagram NAND gate using CMOS logic:

Result: NAND gate

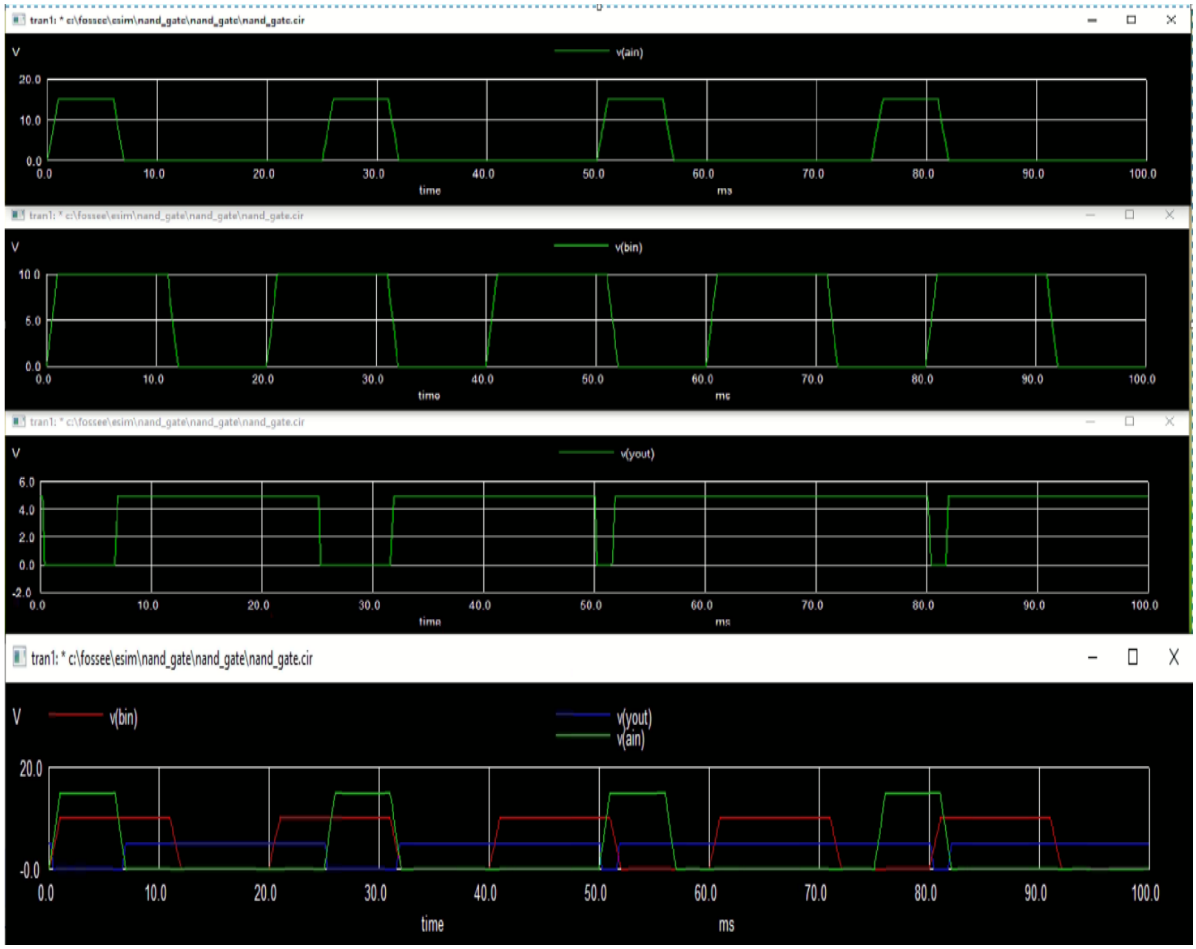


Figure 11 Output waveform of OR gate in simulator

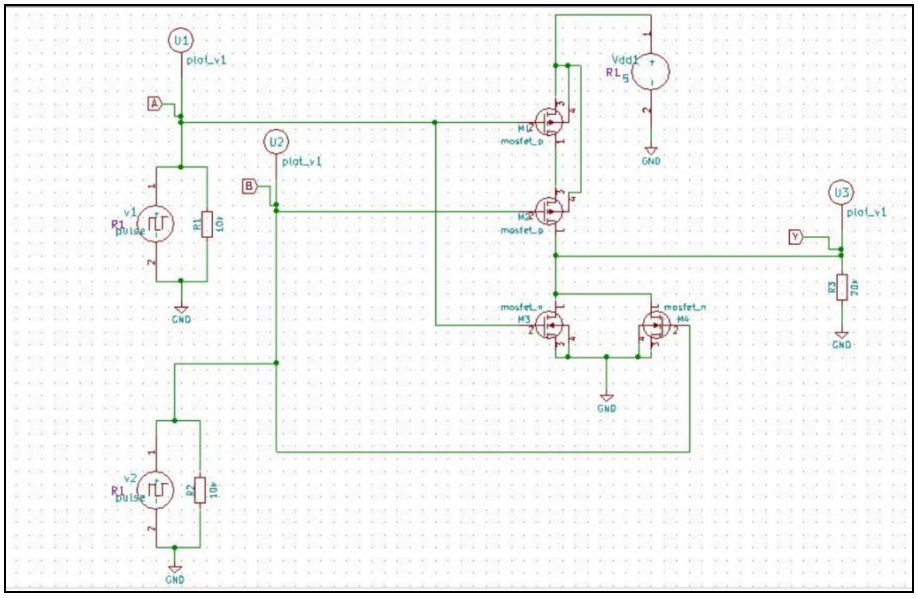


Figure 12 Circuit diagram NOR gate using CMOS logic:

Result:

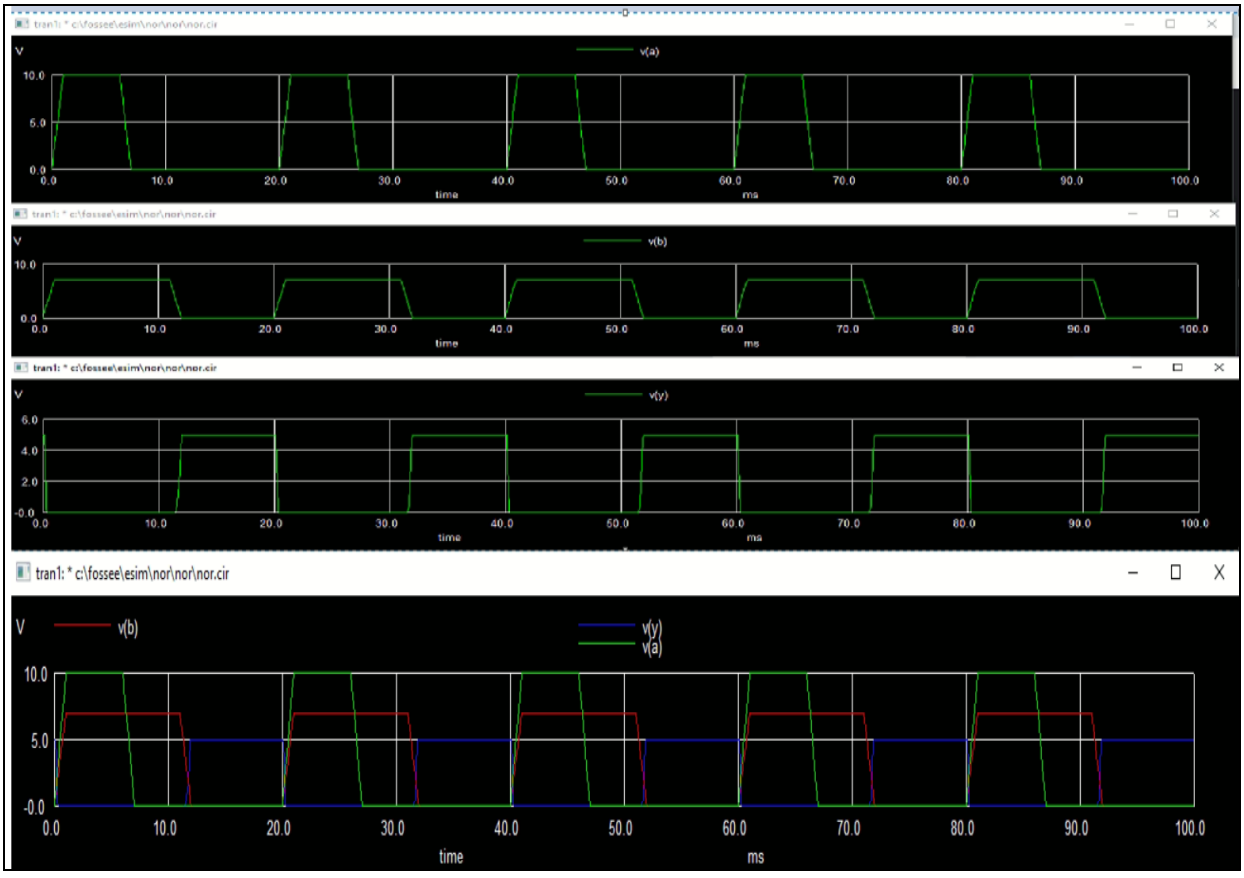


Figure 13 Output waveform of OR gate in simulator

Conclusion : Basic logic gates have been design using e Sim Tool and LT spice

Experiment 2

AIM : Design and implementation of Half adder and Full adder using CMOS logic.

Tool Used : e - Sim and LTspice

Theory:

Half Adder:

There are two inputs and two outputs in a Half Adder. Inputs are named as A and B, and the outputs are named as Sum (S) and Carry (C).

A	B	Sum (S)	Carry (C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

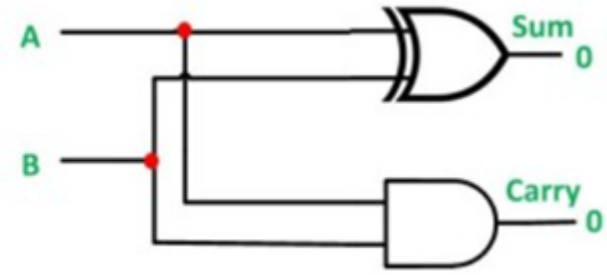


Figure 2.1: Circuit diagram and truth table of Half adder

$S = A \oplus B$ ..... Sum

$S = \bar{A}B + A\bar{B}$

Let $\bar{S} = \overline{\bar{A}B + A\bar{B}}$

$\therefore \bar{\bar{S}} = \bar{A}\bar{B} + AB$ .....implement as pull down network (nMOS)

$\bar{S}_{dual} = (\bar{A} + \bar{B}).(A + B)$ .....Implement as pull up network (pMOS)

$C = A.B$ ..... Carry

Let $\bar{C} = \overline{A.B}$ .....implement as pull down network (nMOS)

$\bar{C}_{dual} = \bar{A} + \bar{B}$ .....Implement as pull up network (pMOS)

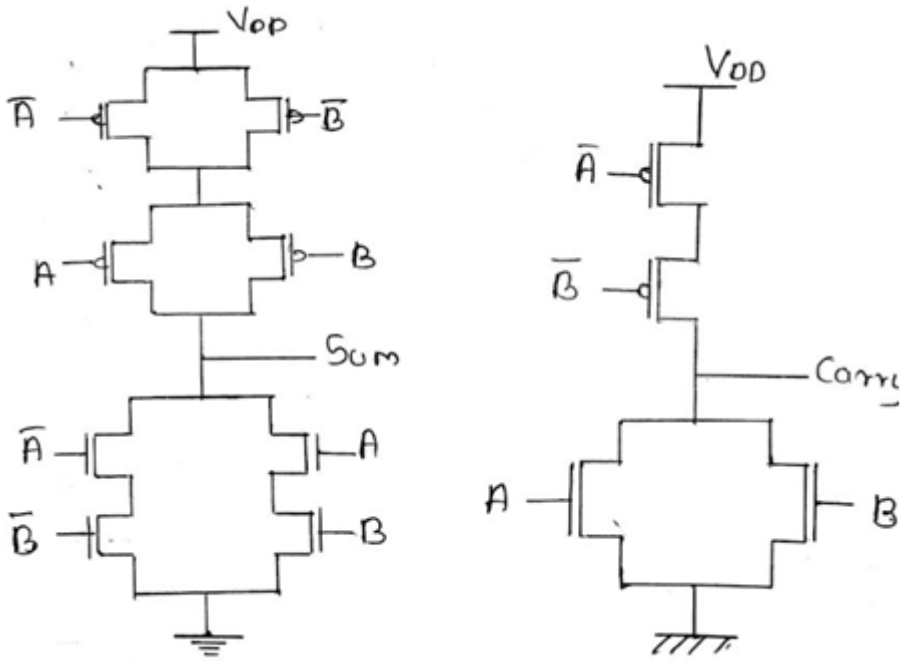
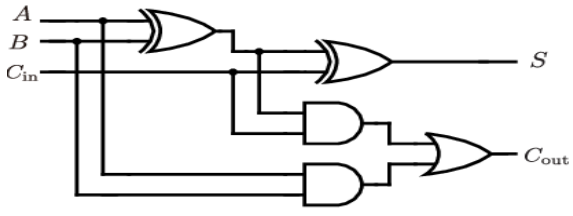


Figure 2.2: CMOC logic diagram of half adder

Full Adder :

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. we use a full adder because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit results.



Inputs			Outputs	
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 2.3: Circuit diagram and truth table of Full adder

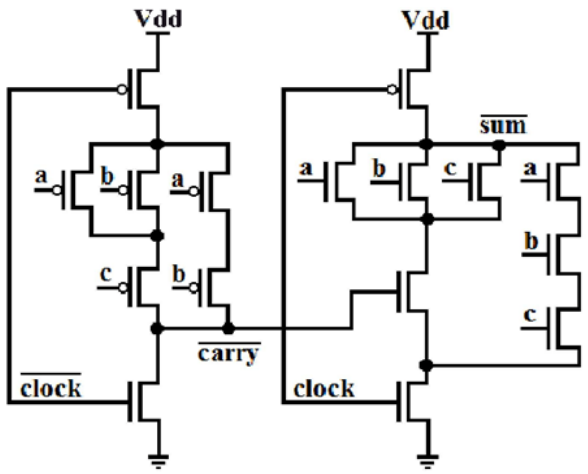


Figure 2.4:CMOS logic diagram of Full adder

Circuit diagram : On Simulator

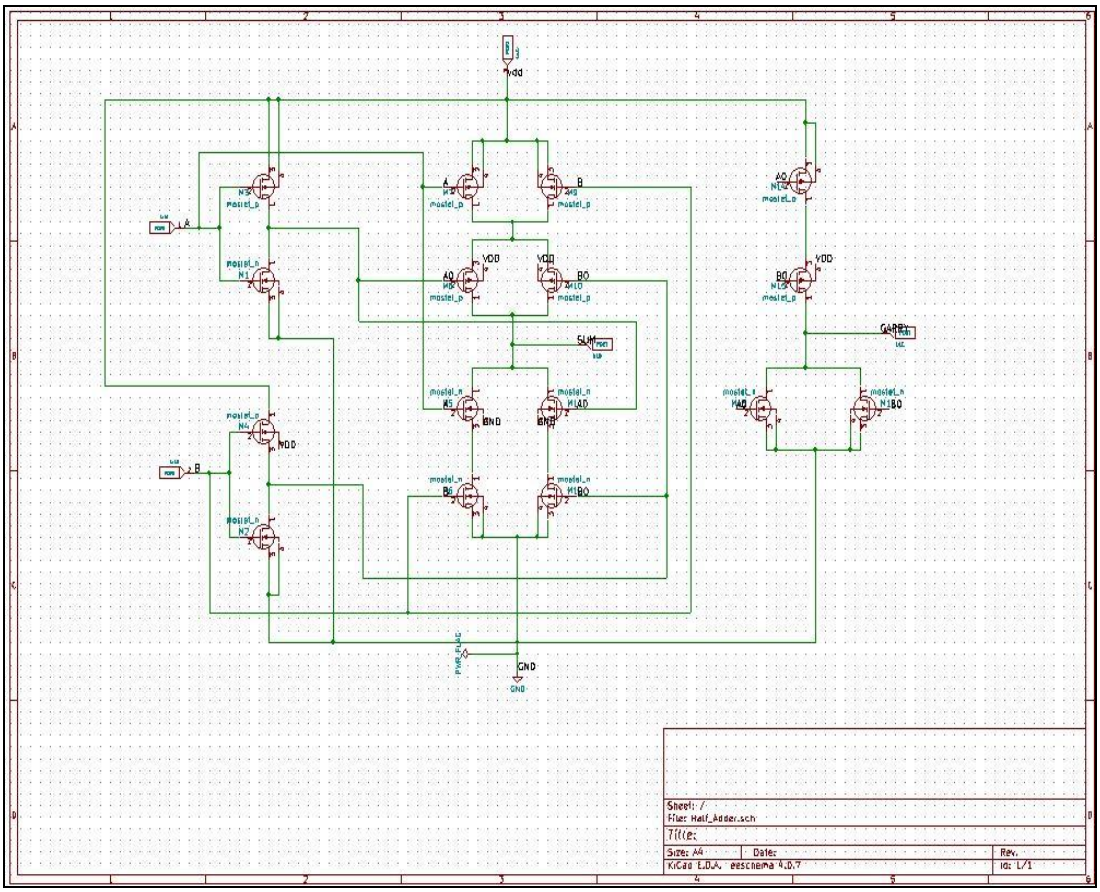


Figure 2.5:CMOS circuit diagram of half Adder

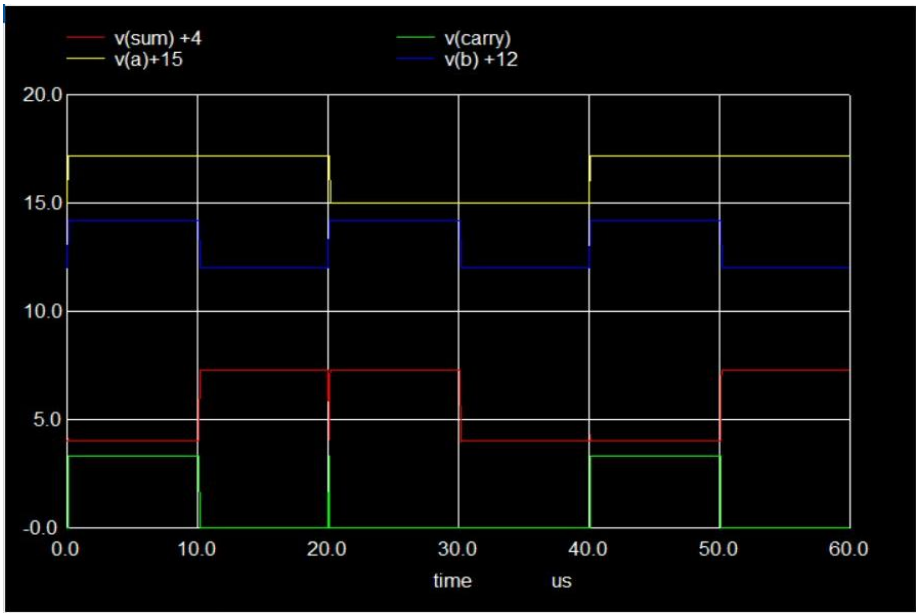


Figure 2.6: Waveform of half adder

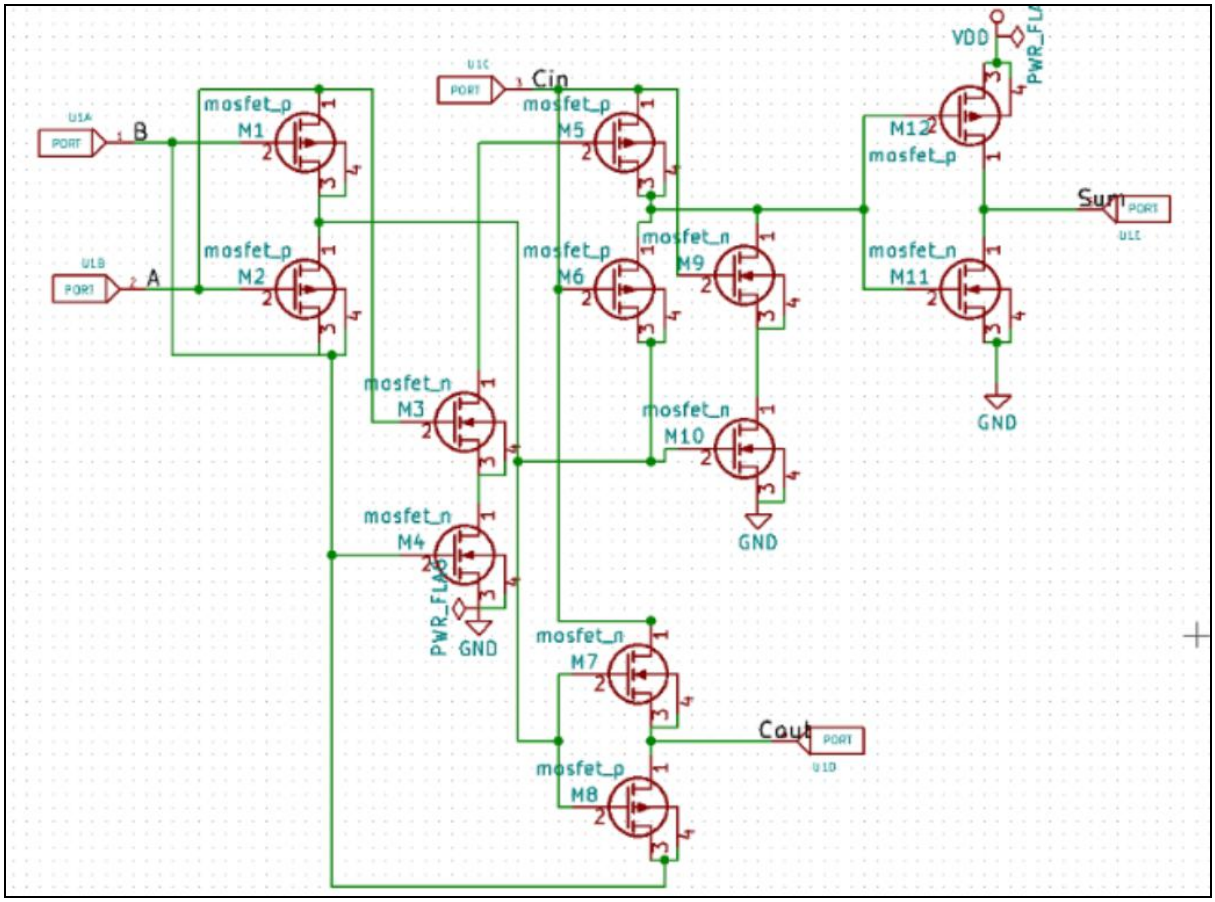


Figure2.7 : Full Adder Circuit diagram.

Output wave form of Full adder

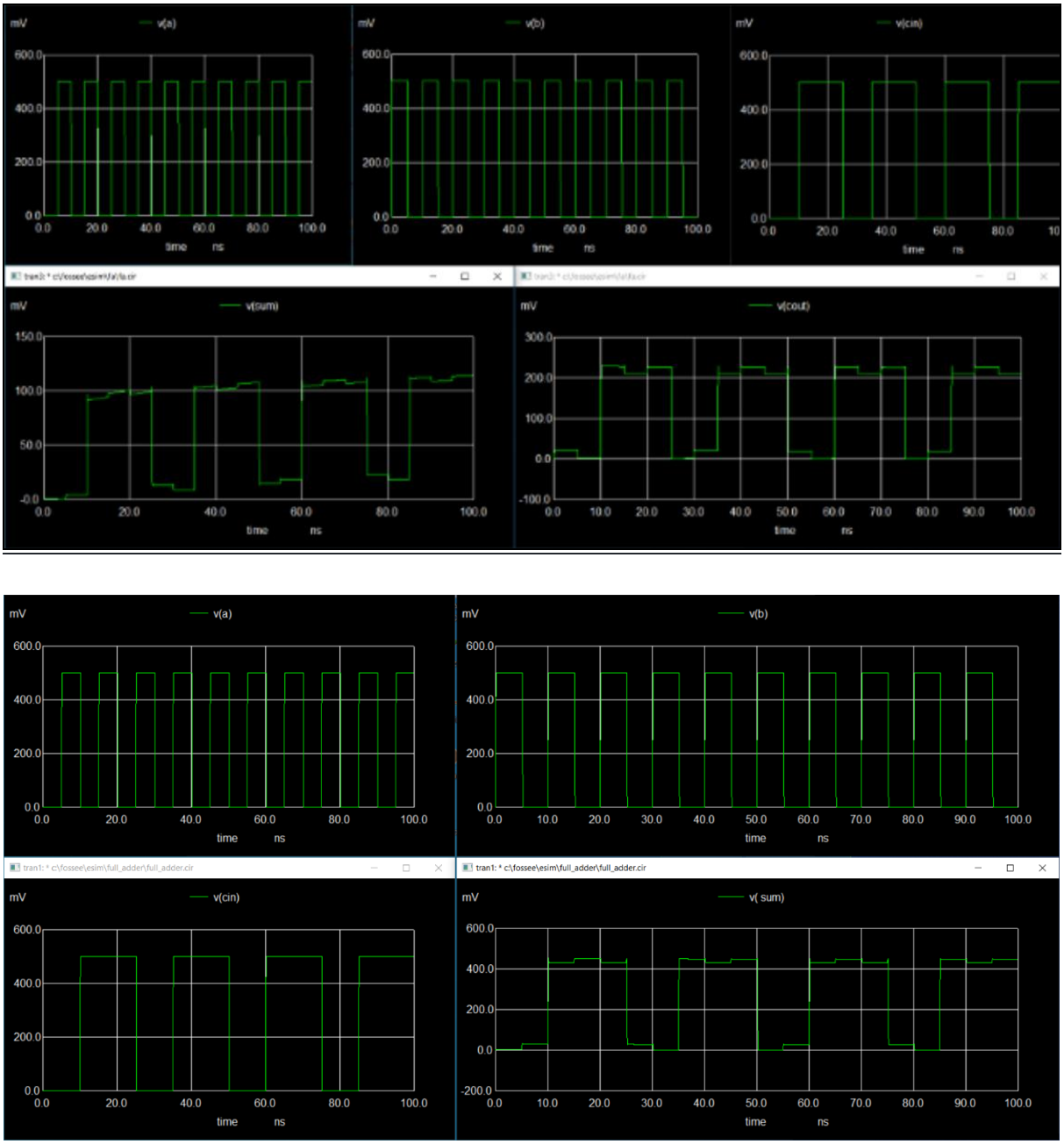


Figure 2.8 Output wave form of Full adder

Result .Half adder and full adder have been verified using tool.

Experiment 3

AIM To simulate the schematic of the common drain amplifier.

Tool used: e-sim and Lt spice

Theory:

The Common drain amplifier is a single transistor MOSFET amplifier, one of the basic fundamental MOSFET amplifiers.The Common drain amplifiers are different from Common source amplifiers where the resistor connected across the drain.
Let us analyze the input resistance, output resistance, and the gain of the amplifier. Based on these parameters, it provides insight into how the circuit will interact with other components.

To determine the input resistance, apply the test voltage at input and measure the current flowing out of it.

Voltage source VIN connected to the gate, (gm) (vgs) voltage-dependent current source at the source terminal. When the input voltage is zero, the flow of the current is zero.

Rin= Voltage test/Current test=Infinite

The input resistance is equal to infinity.

To determine the voltage gain of the amplifier, we must determine the output voltage over the input voltage. We represent the Common drain amplifier in the form of a small-signal model.

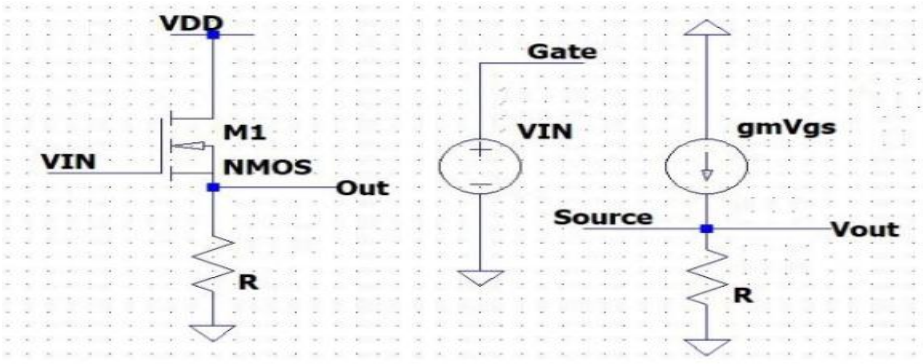


Figure 3.1: Common Drain Amplifier small signal model

Voltage applied across the gate and source terminals, source of the MOSFET connected to the resistor, and connected to ground. Drain of the MOSFET connected to Vdd, and constant voltage across Vdd of the MOSFET would become small-signal ground. Since the voltage is constant across Vdd, there is no change with respect to the function of time, and consider it as ground.

The voltage drop across the resistor must be equal to the current flowing into it.

Vout= (gm) (vgs) (R)

Vgs=Vg-Vs

Vg is the input voltage applied to the circuit, and Vs is the voltage across the source, the same as the voltage across Vout.

Vout=gm (Vin-Vout) R

Vout/Vin= (gm) (R)/ (1+gmR)

When the value of (gm) (R) approaches infinity, then gain will be positive.

The Common drain amplifier would be a good buffer, which prevents the signal source being affected.

To determine the output resistance of the circuit.

The input voltage applied to the gate terminal, the source terminal connected to the voltage-dependent current source and resistance R. Apply test voltage across source resistor and measure the current across the resistor and short all the independent source.

Test Current= (Test Voltage/ Resistor)-(gm) (vgs)

Vgs=-Vtest

Test Current=-Vtest (1/Resistor + gm)

Rout= (R/ (1+gmR)

Circuit Simulation using LTSpice

Let's start the circuit simulation using LTSpice, to open a new schematic editor. Go to File, select the New schematic. Components required to design a Common Drain Amplifier are NMOS, voltage source, wire, and ground. Now place the NMOS in the schematic, click on to the component symbol, and you would get the select component symbol popup from the list select the NMOS. Draw the Common Drain Amplifier schematic as shown in figure below, we will convert this circuit into a symbol.

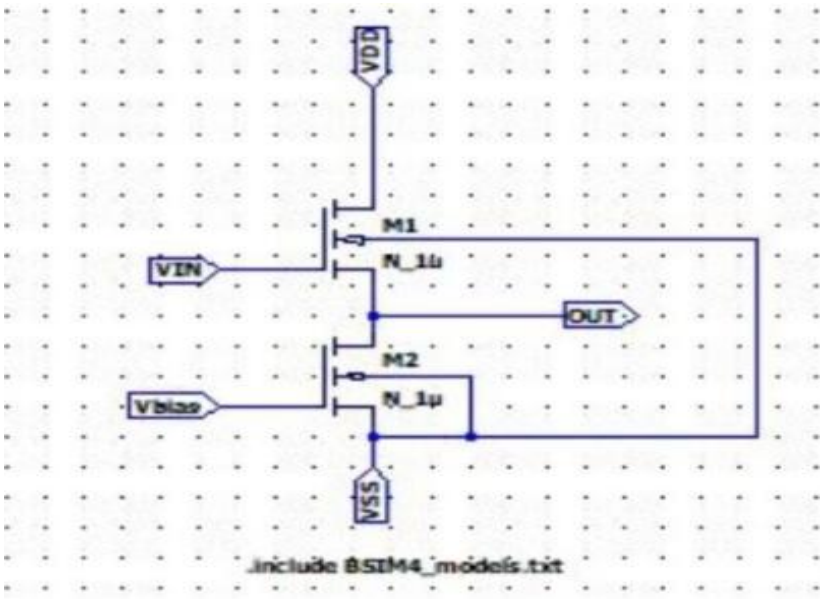


Figure 3.2 Common Drain Amplifier schematic

Result:

Run the simulation to plot the DC Sweep and the transient analysis of the Common Drain Amplifier. The simulation results is shown in the figure below

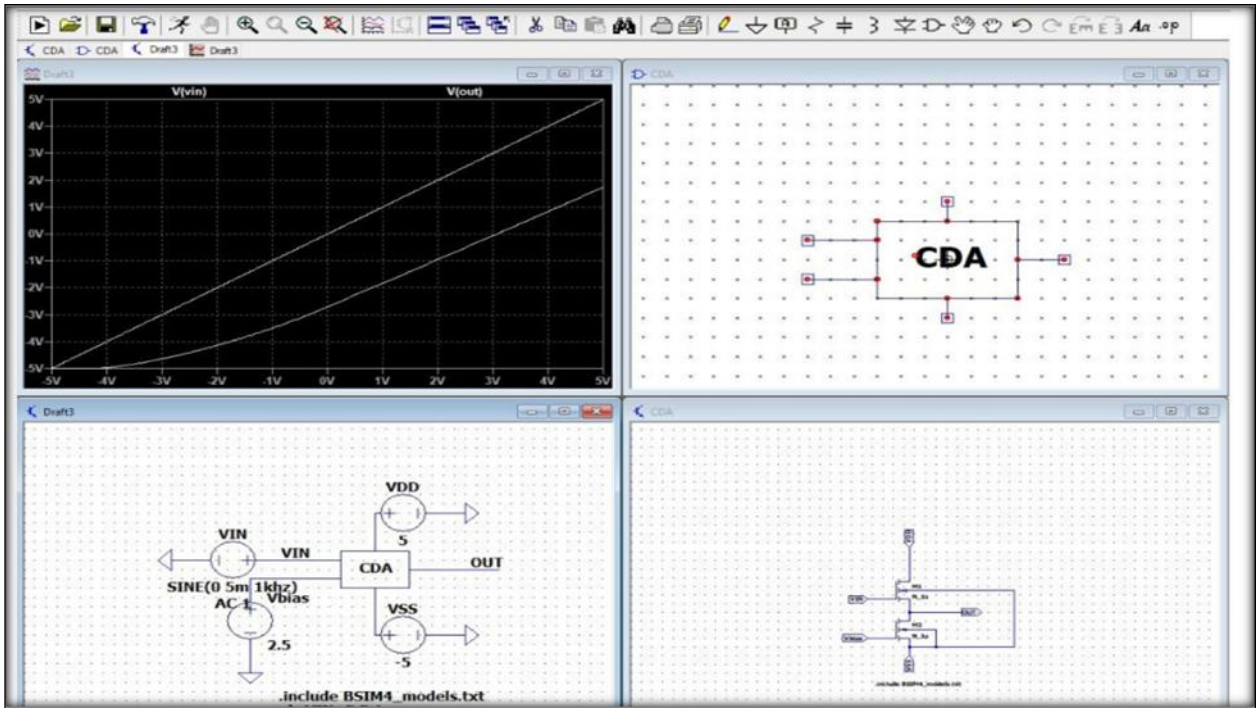


Figure 3.3 : DC analysis

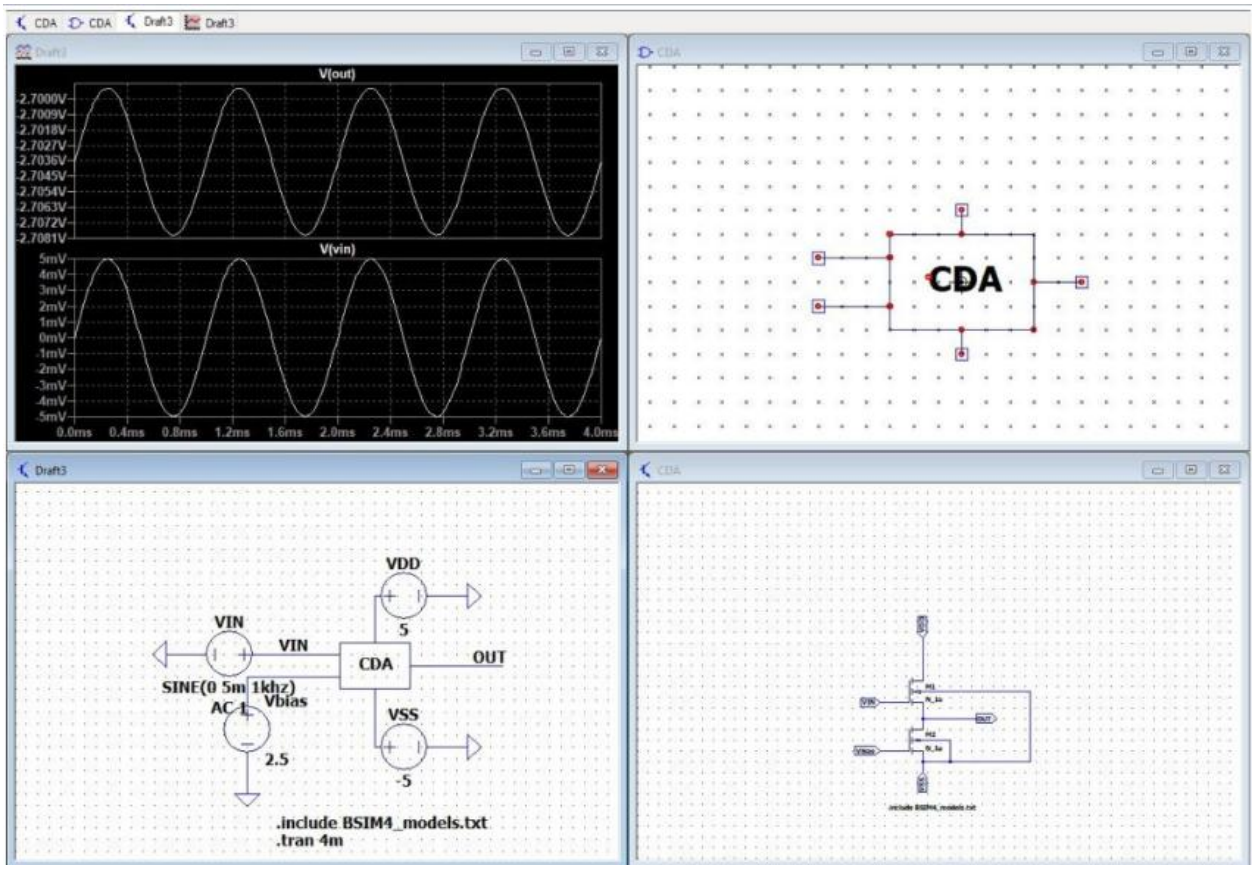


Figure 3.4: Transient analysis

Experiment 4

AIM: To simulate the schematic of the differential amplifier.

Tool used: e-sim and Lt spice

Theory:

Differential amplifier is the fundamental building block in the CMOS analog integrated circuit design.

There are three different types of differential amplifier

1) Source coupled pair

2) Source cross-coupled pair

3) Current differential amplifier

The diff-amplifier amplifies the difference between the two input signal applied across the input terminal. The output of the differential amplifier is directly proportional to the difference between the two input signals.

The difference between the input signals of the differential amplifier is known as the differential signals. Thus the output of the difference amplifier will be non-zero only if the differential input signal is non zero.

The differential gain of an amplifier calculation shown below.

VO=Ad (V1-V2)

Vd= (V1-V2)

VO=AdVd

Ad=Vo/Vd

If the applied input voltage is differential or they are out of phase with each other. V1 is a sinusoid signal biased at 2.5V with an amplitude of 5mv.

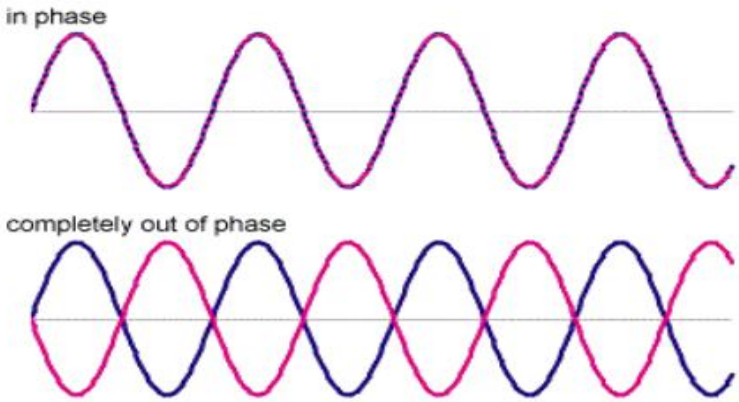


Figure 4.1 : Waveform ofdifferential amplifier.

Differential Amplifier Circuit Generator using E sim

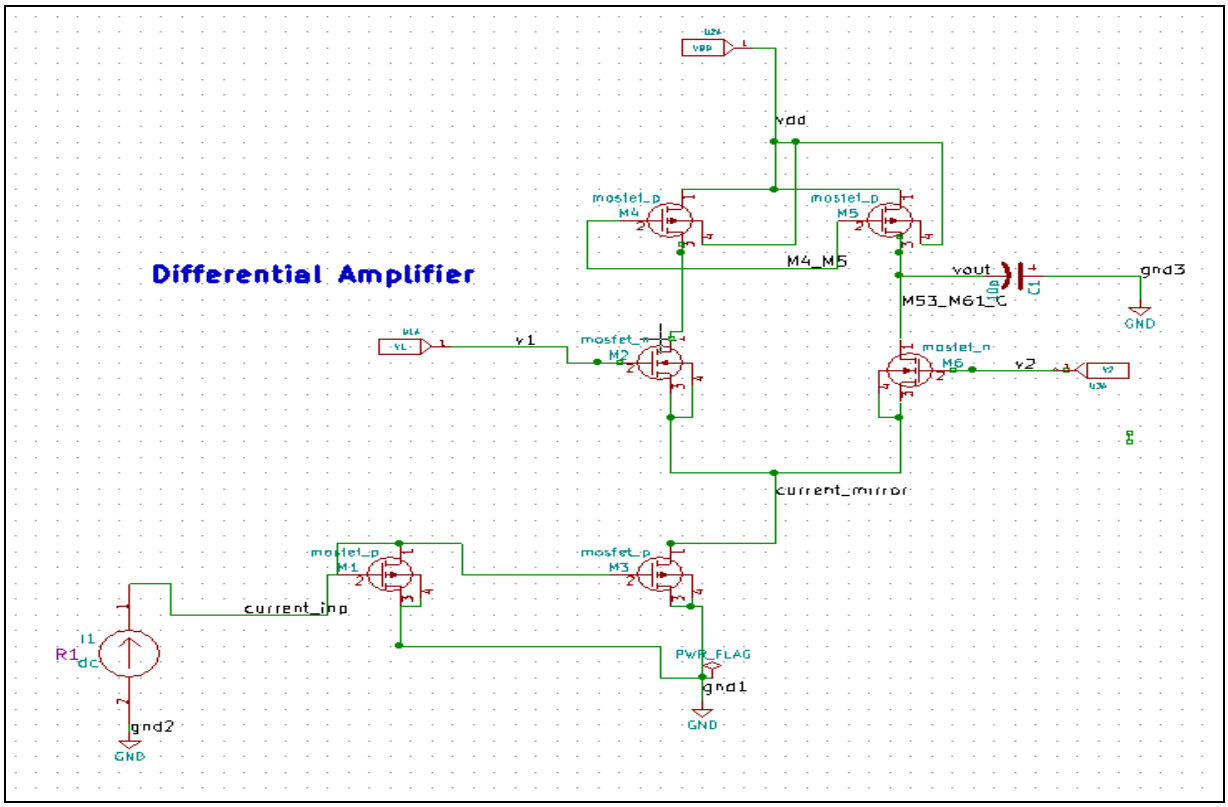


Figure 4.2 : Circuit diagram ofdifferential amplifier.

Result: Output waveform of Differential amplifier

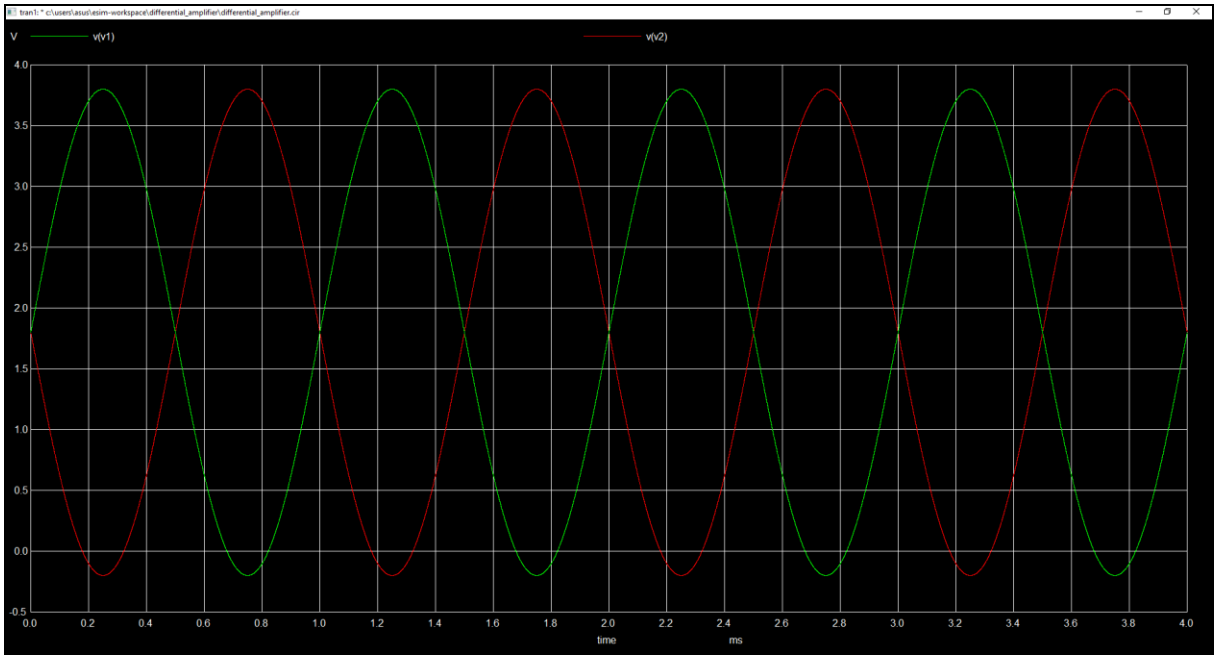


Figure 4.3 : Output waveform of Differential amplifier

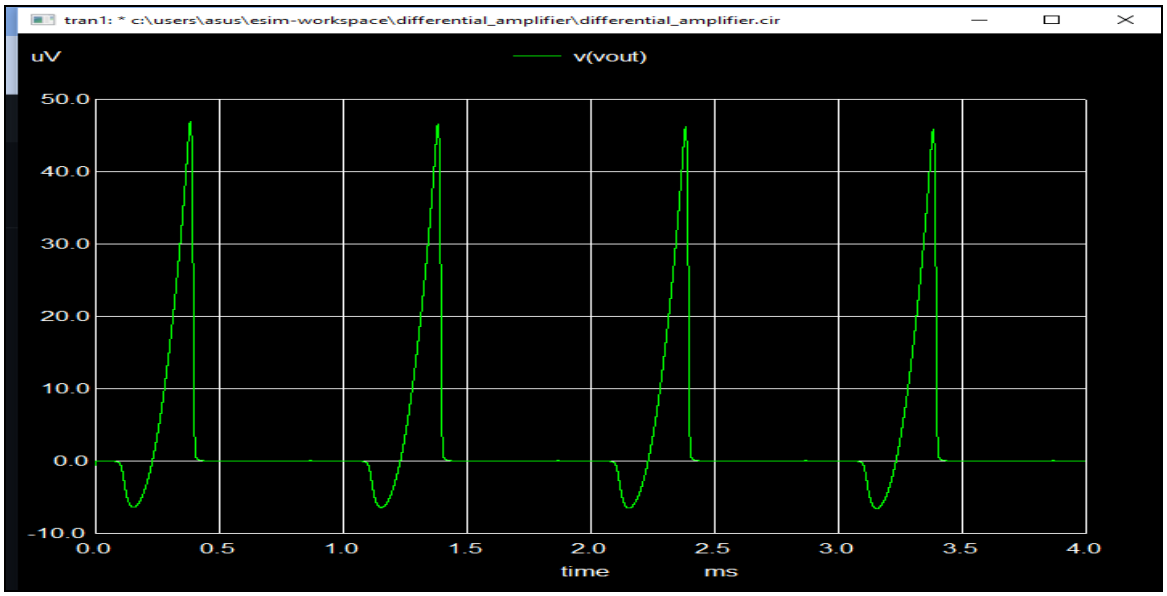


Figure 4.4 : Output waveform of Differential amplifier

Experiment 5.

AIM To simulate the schematic of the 2-Stage Operational Amplifier.

Tool used: e-sim and Lt spice

Theory: Op-amps can be divided into two types according to the manufacturing process used: CMOS and bipolar. Since CMOS op-amps are voltage-controlled devices, they operate with low DC input bias current (I_I) and therefore their power consumption is low. An operational amplifier generally consists of three stages, anmely,1. a differential amplifier 2. additional amplifier stages to provide the required voltage gain and dc level shifting 3. an emitter- follower or source follower output stage to provide current gain and low output resistance.

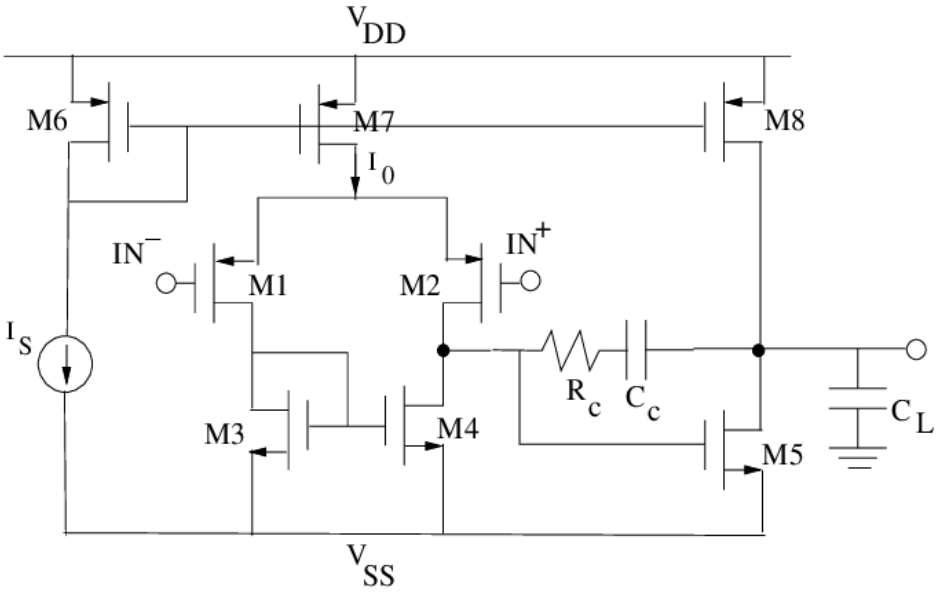


Figure: 5.1 Two-stage operational amplifier

A two-stage operational amplifier consists of a differential amplifier at the. input stage, while the second stage is a high gain stage biased by the output of the differential amplifier.

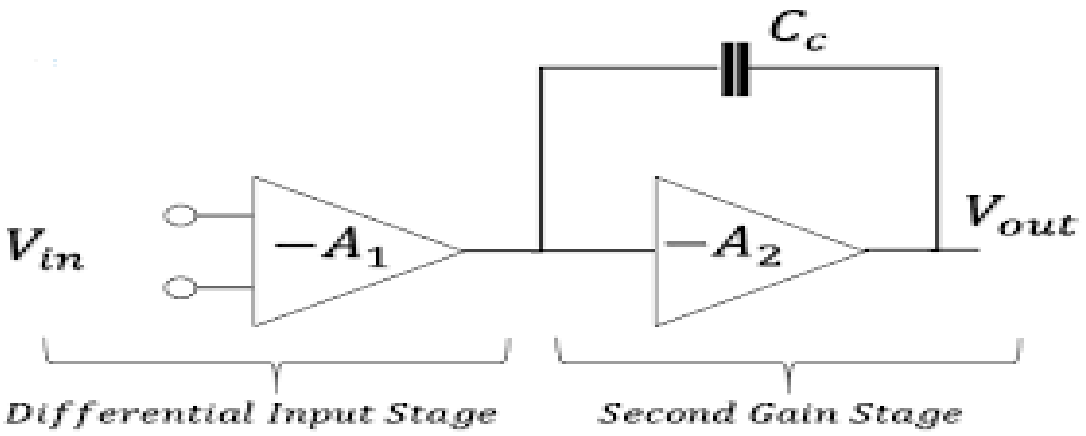


Figure: 5.2 Two-stage operational amplifier

Circuit diagram:

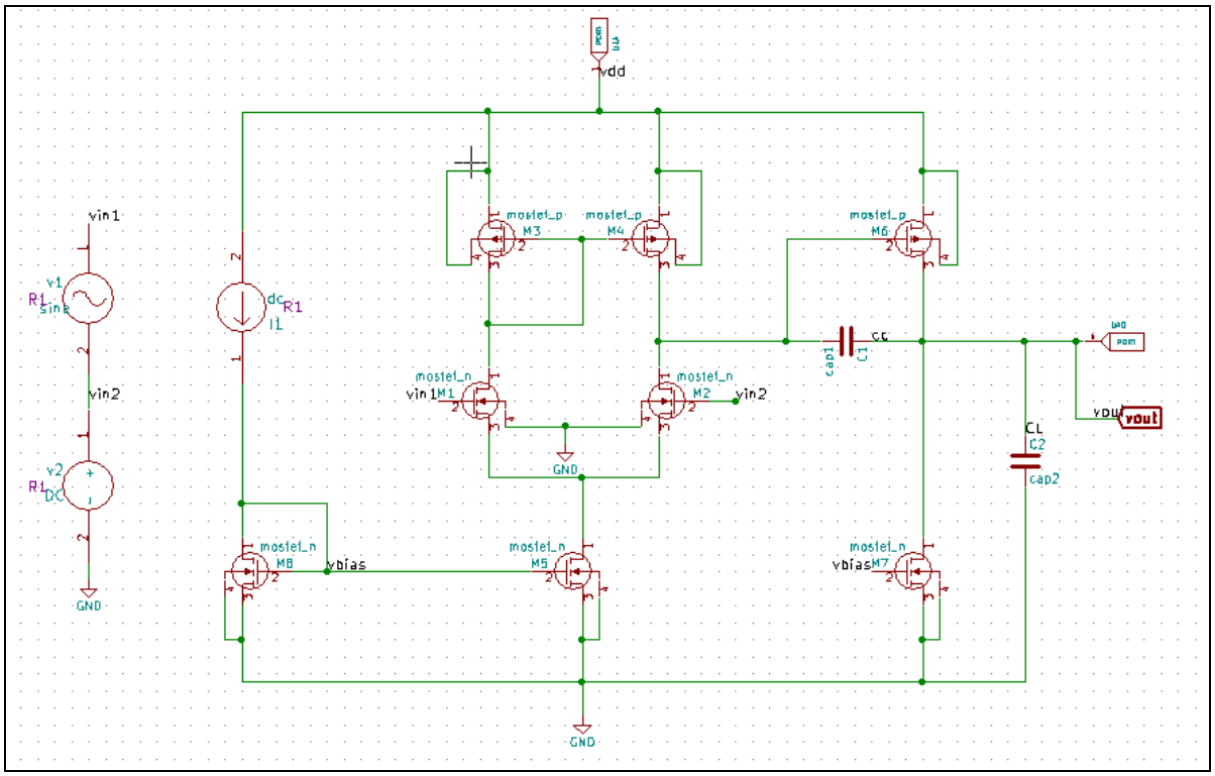


Figure: 5.3 Two-stage operational amplifier

Result:

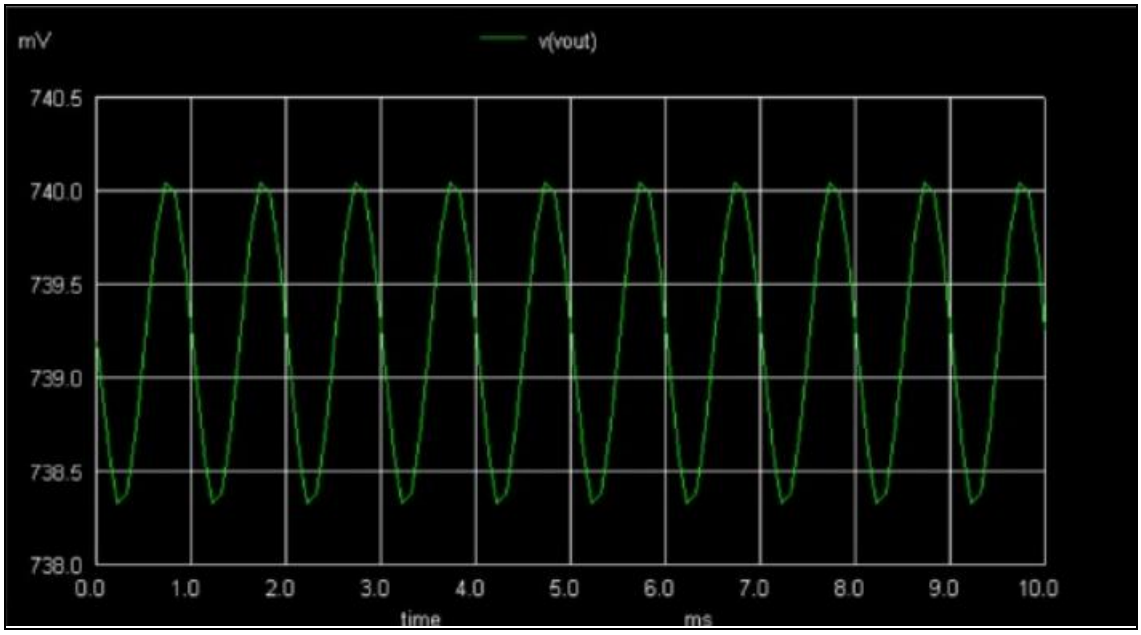


Figure: 5.4 Two-stage operational amplifier

Experiment : 6

AIM: Design of 2-4 decoder using MOS technology

Tool used: e-sim and LT spice

Theory: Decoder is a combinational circuit that has 'n' input lines and maximum of 2^n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of 'n' input variables lines, when it is enabled. 2 to 4 Decoder

Let 2 to 4 Decoder has two inputs A_1 & A_0 and four outputs Y_3, Y_2, Y_1 & Y_0. The block diagram of 2 to 4 decoder is shown in the following figure.

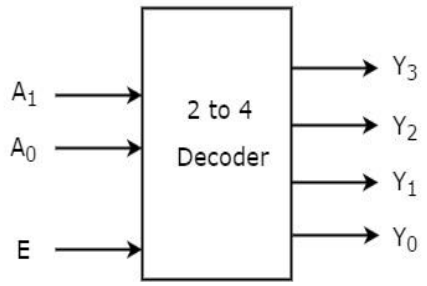


Figure: 6.1 Logic symbol of Decoder

One of these four outputs will be '1' for each combination of inputs when enable, E is '1'. The Truth table of 2 to 4 decoder is shown below.

Truth table of 2 to 4 decoder is shown below.

Enable	Inputs		Outputs			
E	A_1	A_0	Y_3	Y_2	Y_1	Y_0
0	x	x	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

From Truth table, we can write the **Boolean functions** for each output as

From Truth table, we can write the **Boolean functions** for each output as

$$Y_3 = E.A_1.A_0$$

$$Y_2 = E.A_1.A_0{}'$$

$$Y_1 = E.A_1{}'.A_0$$

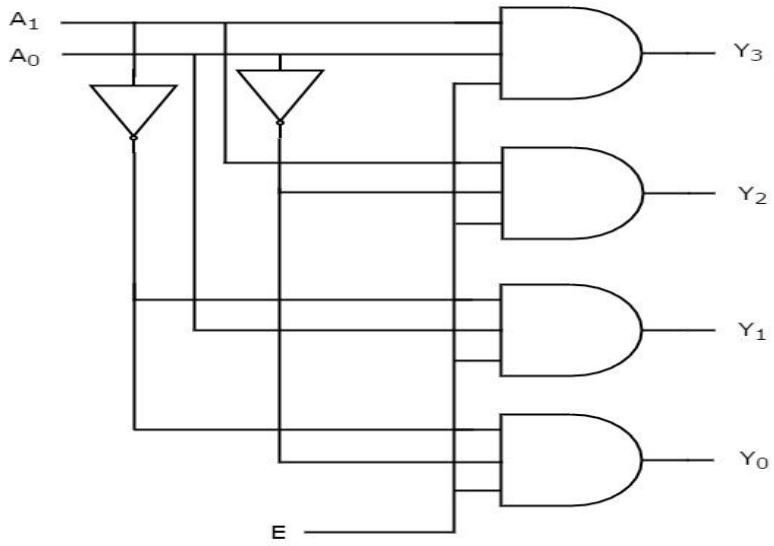
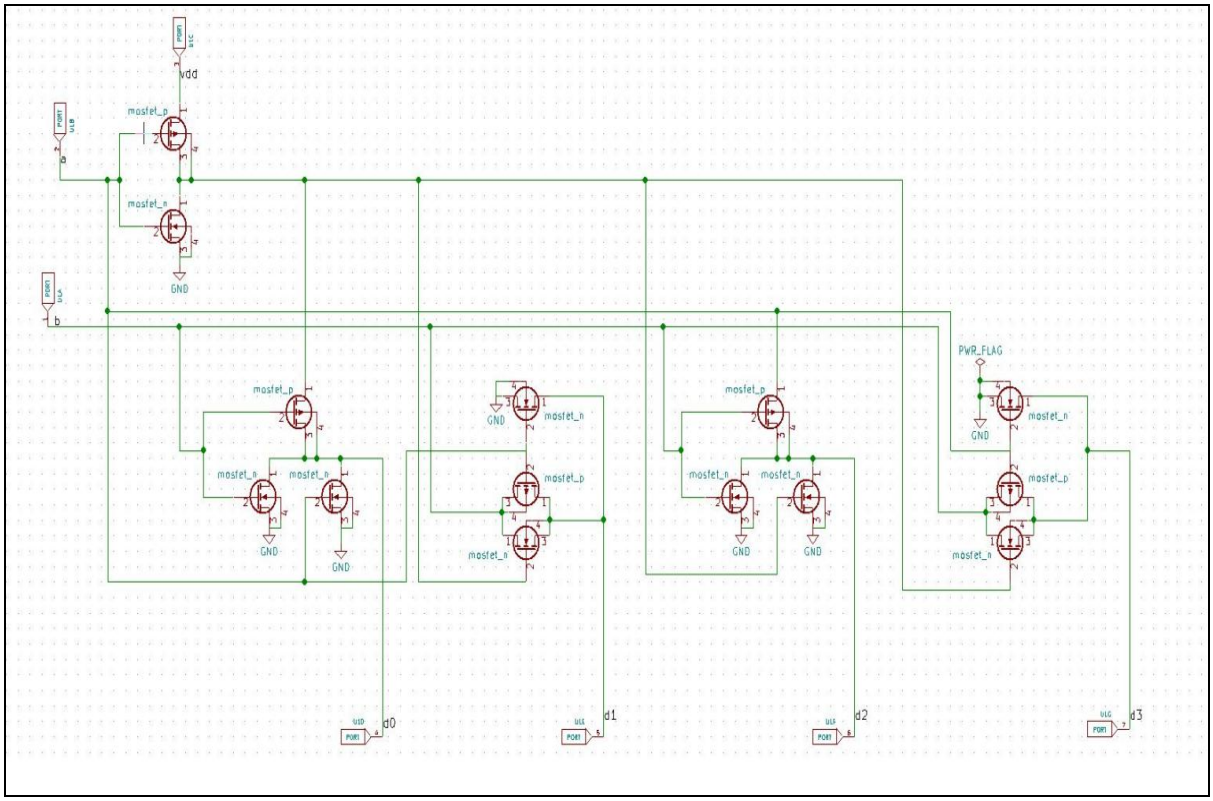


Figure: 6.2 Logic diagram of Decoder

Circuit diagram



Result:

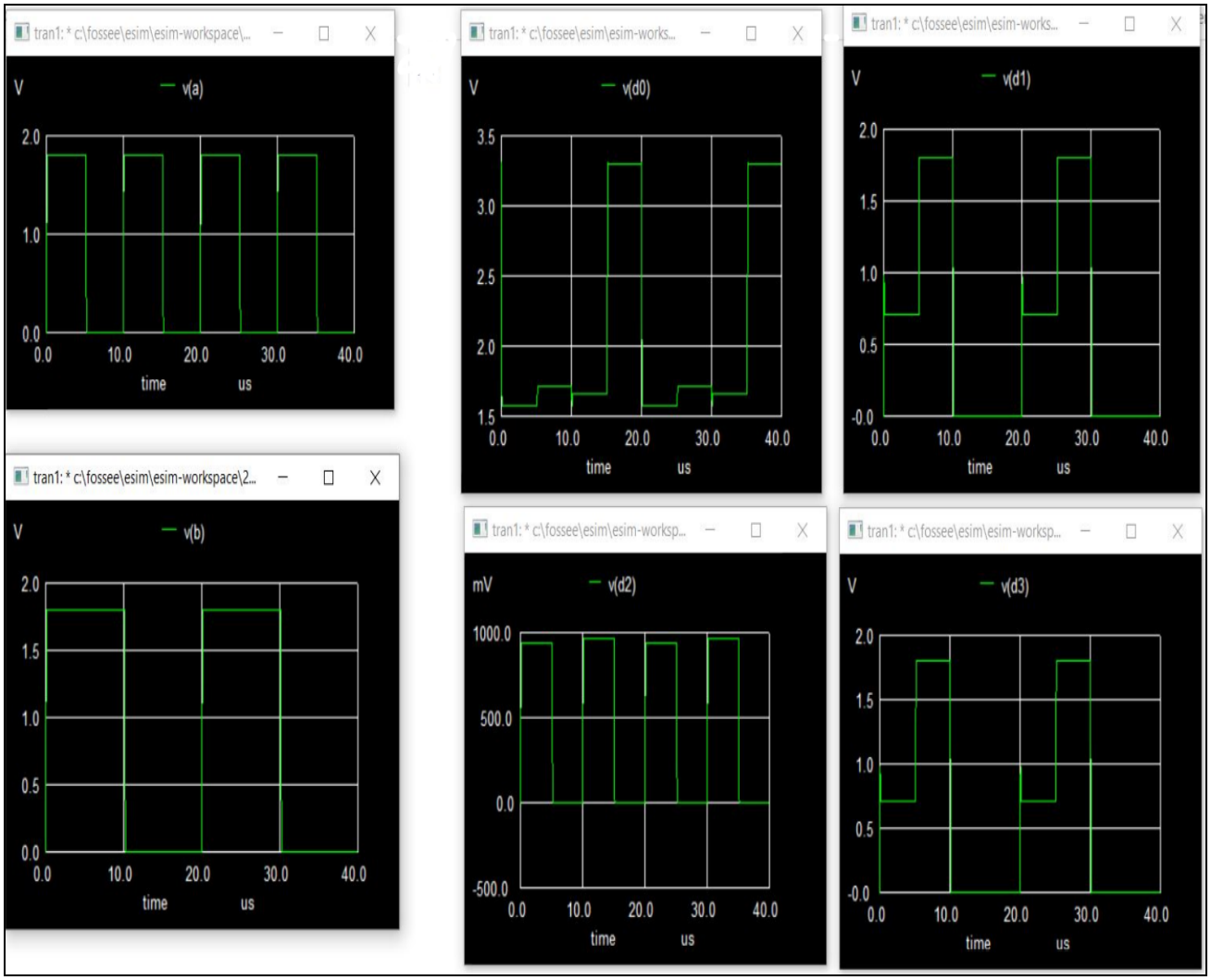


Figure: 6.3 Output waveform of Decoder

Experiment : 7

AIM: Design of 4:1 mux using transmission gate

Tool used: e-sim and LT spice

Theory:

4x1 Multiplexer

4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y. The block diagram of 4x1 Multiplexer is shown in the following figure.

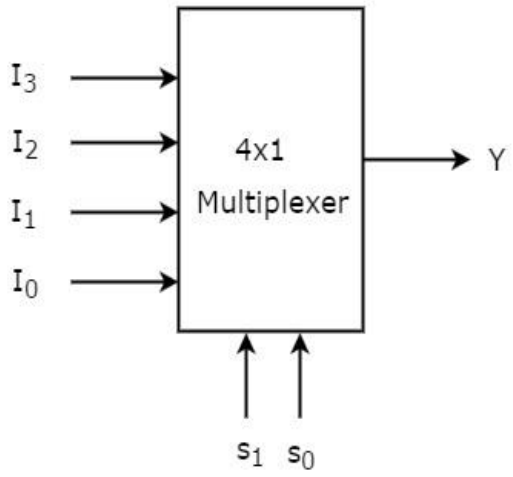


Figure: 7.1 logic symbol of multiplexer

One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. Truth table of 4x1 Multiplexer is shown below.

Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

From Truth table, we can directly write the **Boolean function** for output, Y as

$$Y = S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$$

We can implement this Boolean function using Inverters, AND gates & OR gate. The circuit diagram of 4x1 multiplexer is shown in the following figure.

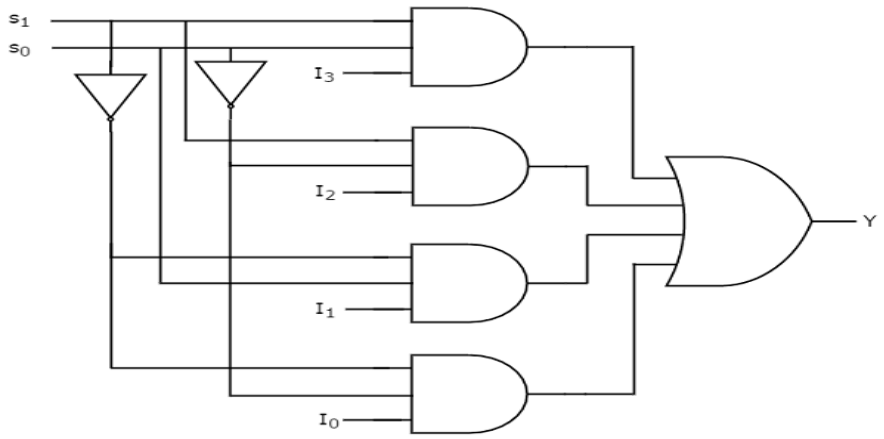


Figure: 7.2 logic diagram of multiplexer

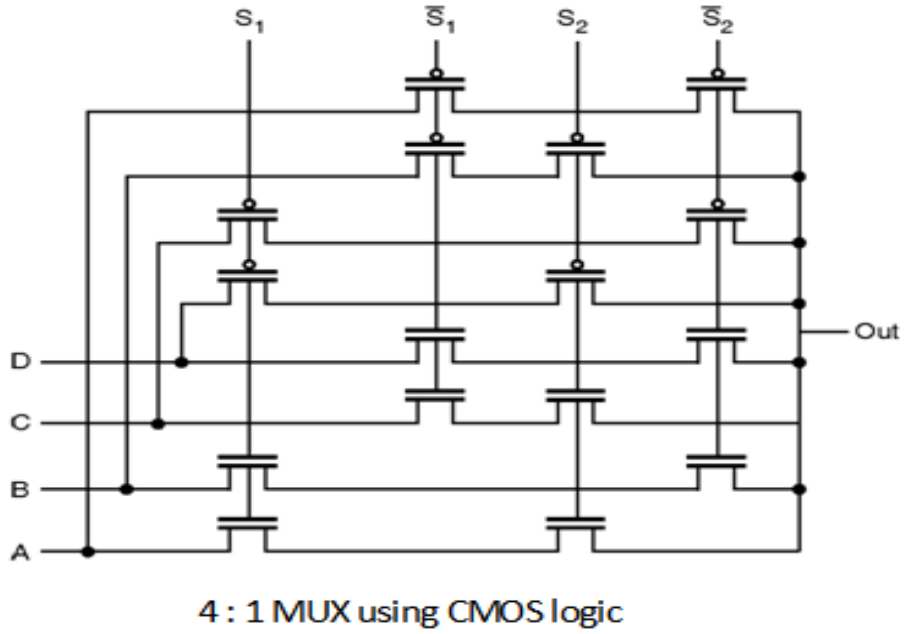


Figure: 7.3 Circuit diagram of 4:1 multiplexer using CMOS logic

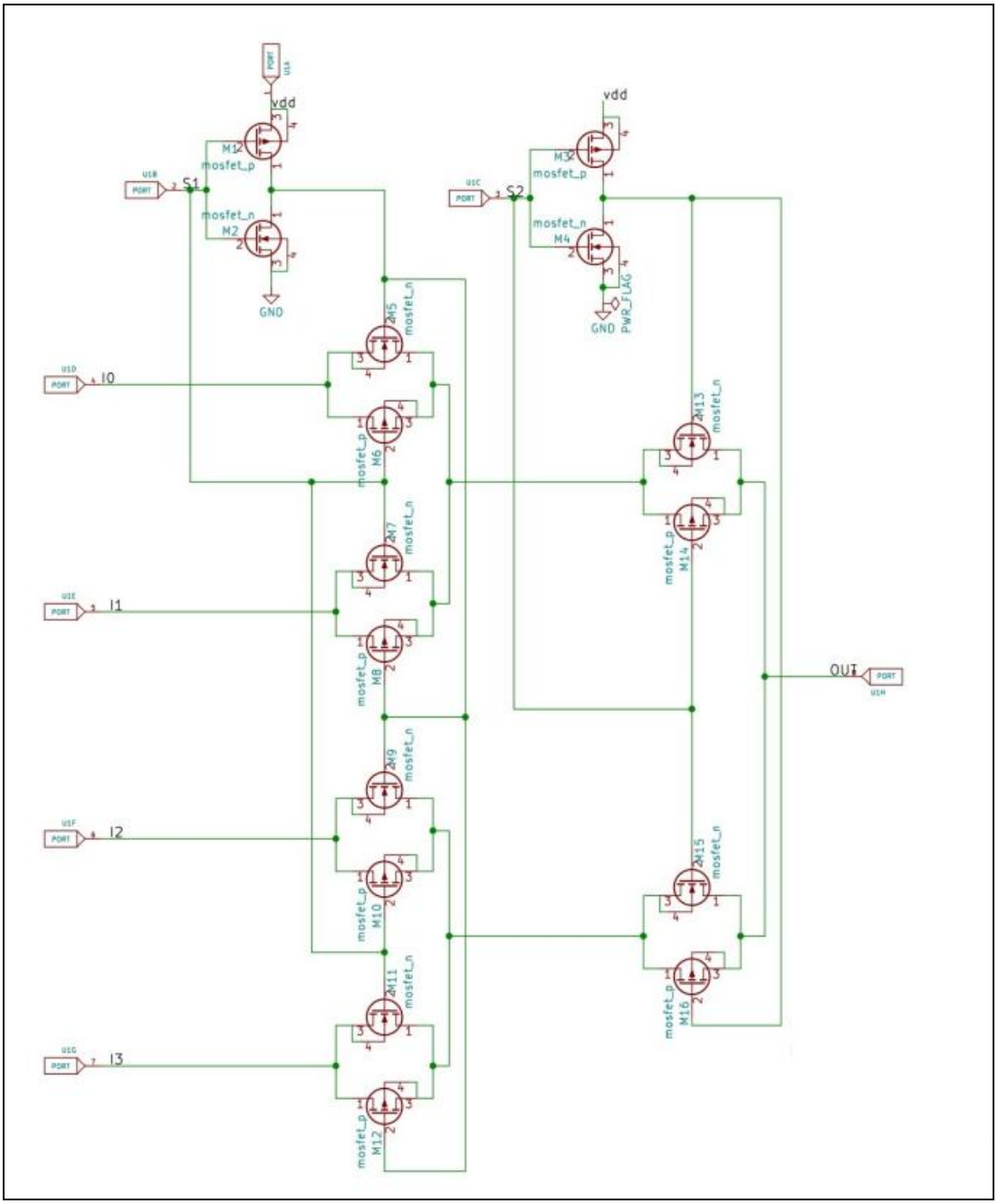


Figure: 7.4 Circuit diagram of 4:1 multiplexer using CMOS logic

Result:

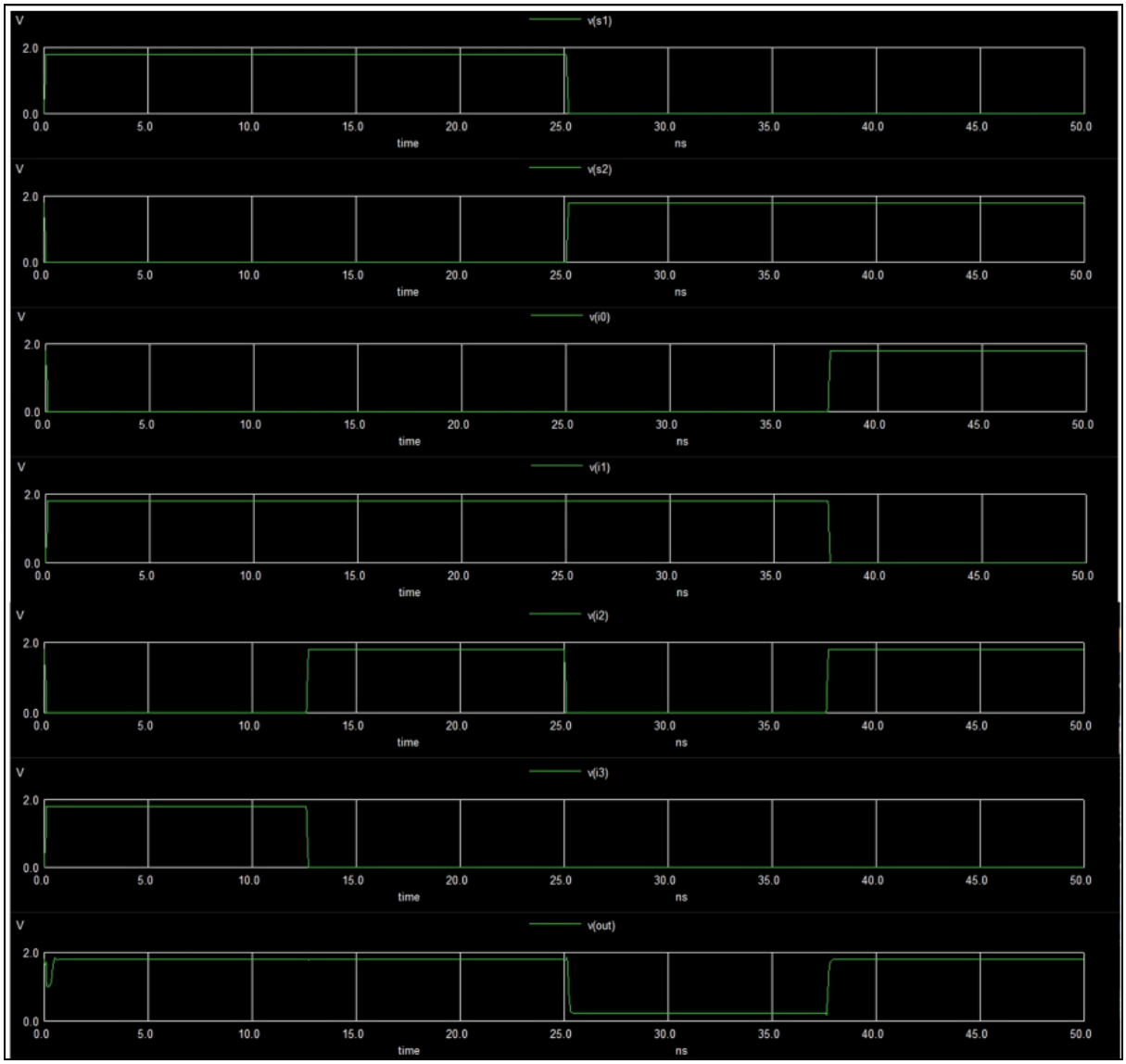


Figure:7.5 Output waveform of 4:1 multiplexer using CMOS logic

Experiment 8

AIM: Design and implementation of Flip flop circuit.

Tool used: e-sim and Lt spice

Theory: In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information – a bistablemultivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. The flip-flops are of the following types:

- S-R Flip Flop.
- J-K Flip Flop.
- T Flip Flop.
- D Flip Flop.

SR Flip-Flop

SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal. The circuit diagram of SR flip-flop is shown in the following figure.

This circuit has two inputs S & R and two outputs Qtt & Qtt'. The operation of SR flip flop is similar to SR Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.

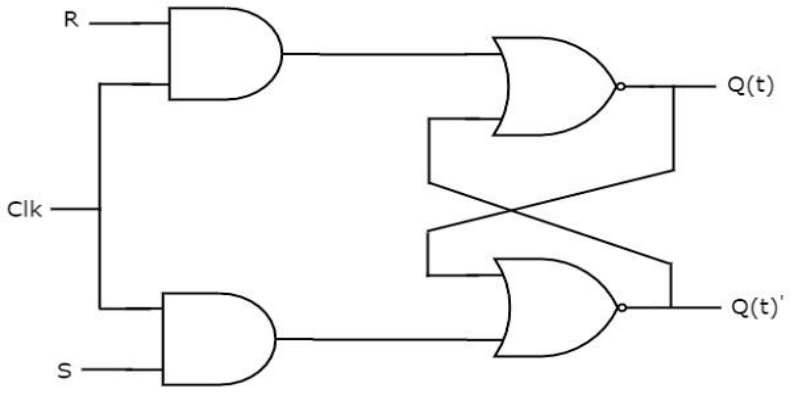


Figure: 8.1 logic diagram S-R flip-flop

The following table shows the state table of SR flip-flop.

S	R	Qt+1
0	0	Qt
0	1	0
1	0	1
1	1	-

Here, Qt & Qt+1 are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive transition of clock signal is applied. The following table shows the characteristic table of SR flip-flop.

Present Inputs		**Present State**	**Next State**
S	**R**	**Q**t	**Q**t+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Circuit Diagram:

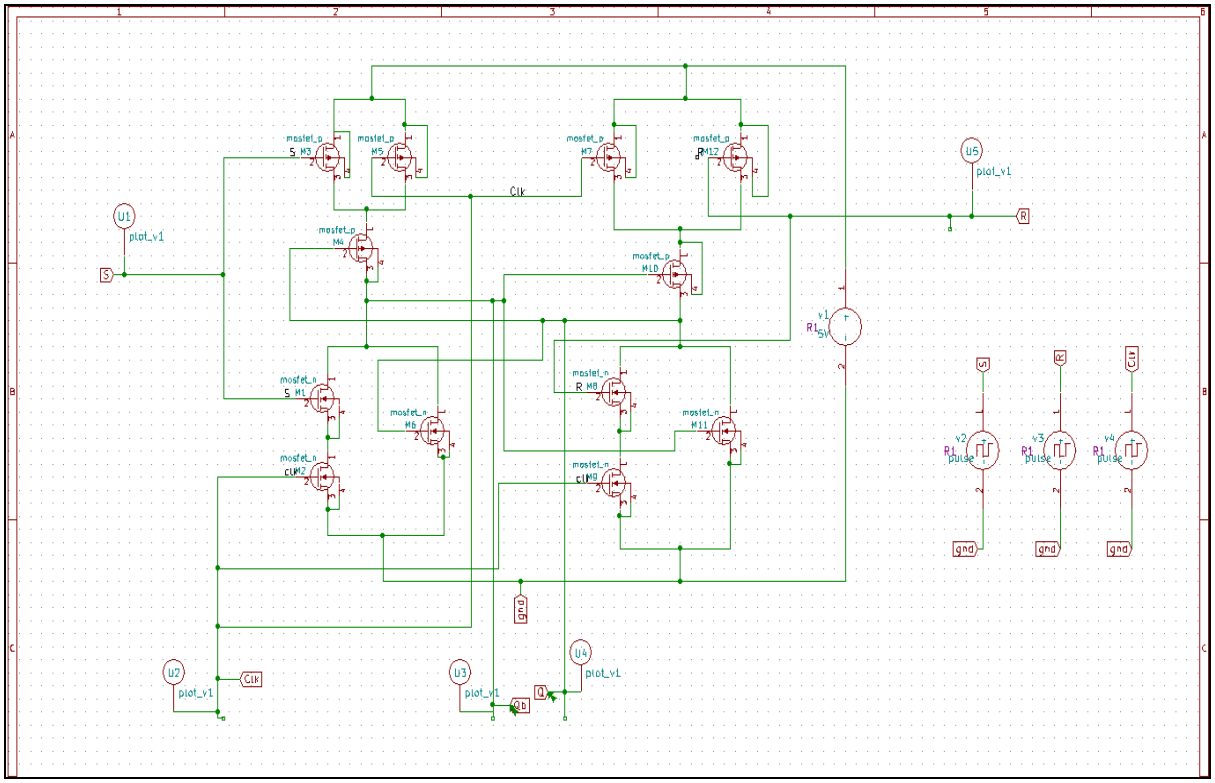


Figure: 8.2 Circuit diagram flip-flop

Result:

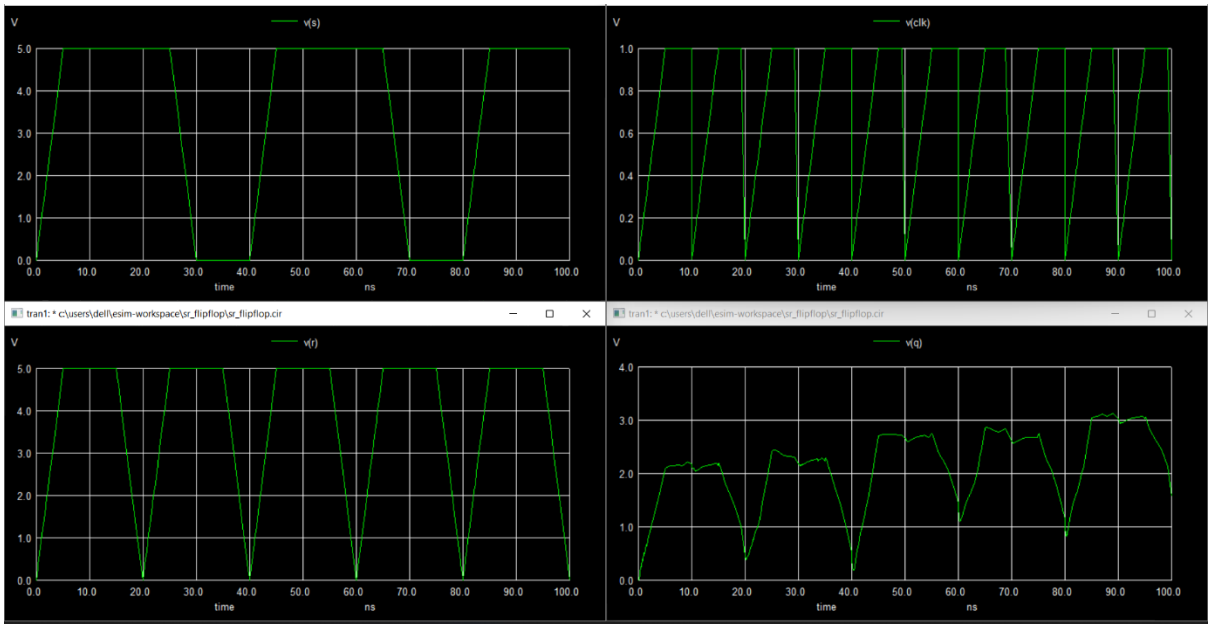


Figure: 8.3 Output waveform of flip-flop

Experiment 9

AIM : Layout design CMOS inverters and its analysis .

Tool used:

Theory:

CMOS Fabrication

CMOS transistors are fabricated on silicon wafer. Lithography process similar to printing pressOn each step, different materials are deposited or etched .Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process.Typically use p-type substrate for nMOS transistors.
Requires n-well for body of pMOS transistors

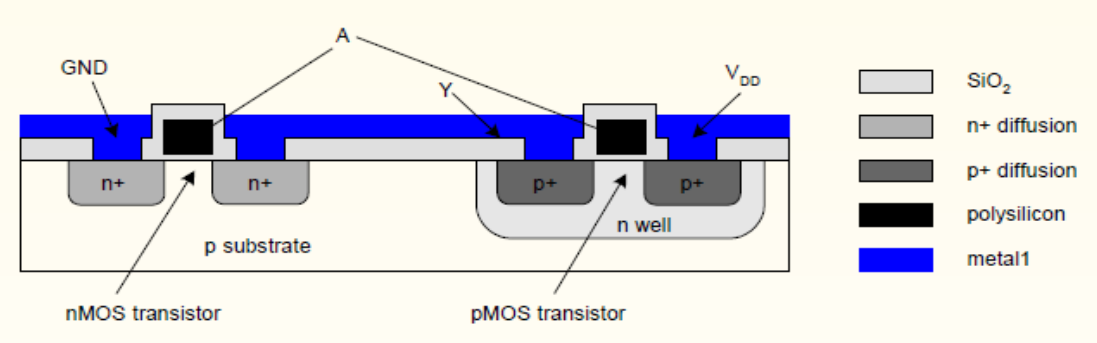


Figure 9.1 CMOS Fabrication

Well and Substrate Taps:

Substrate must be tied to GND, n-well to VDD
(Reverse-biased diodes isolate regions)
Metal to lightly-doped semiconductor forms poor connectioncalled Schottky Diode { use heavily doped well and substratecontacts/taps

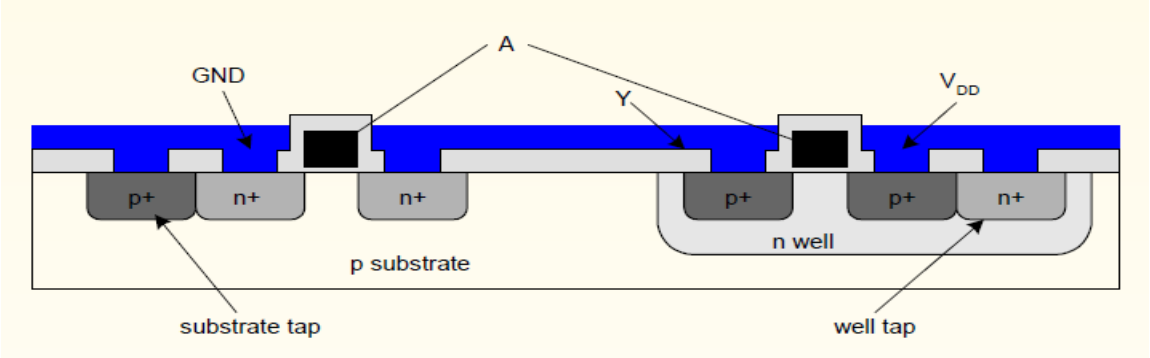


Figure 9.2 CMOS Fabrication

Inverter Masks

Transistors and wires are defined by masks
Cross-sections shown above taken along dashed line.

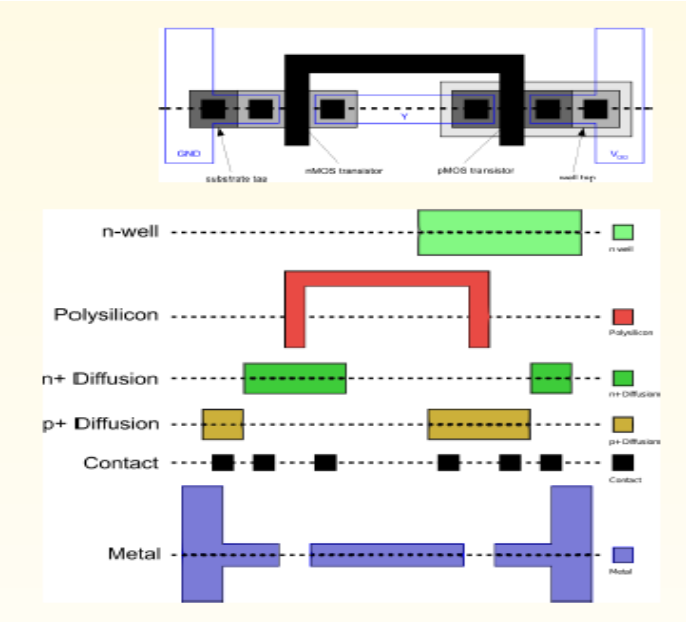


Figure 9.3 Inverter Masks

Layout Design:

- Describes actual layers and geometry on the silicon substrate to implement a function
- Need to define transistors, interconnection
- Transistor widths (for performance)
- Spacing, interconnect widths, to reduce defects, satisfy power requirements
- Contacts (between poly or active and metal), and via(between metal layers)
- Wells and their contacts (to power or ground)
- Layout of lower-level cells constrained by higher-level requirements: floorplanning
- \design iteration"
- Chips are specified with set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain.
- Set by minimum width of polysilicon (= minimum \drawn"gate length)
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms ofλ= f/2 e.g.,λ = 0.3µm in 0.6µm process.

CMOS Inverter Layout

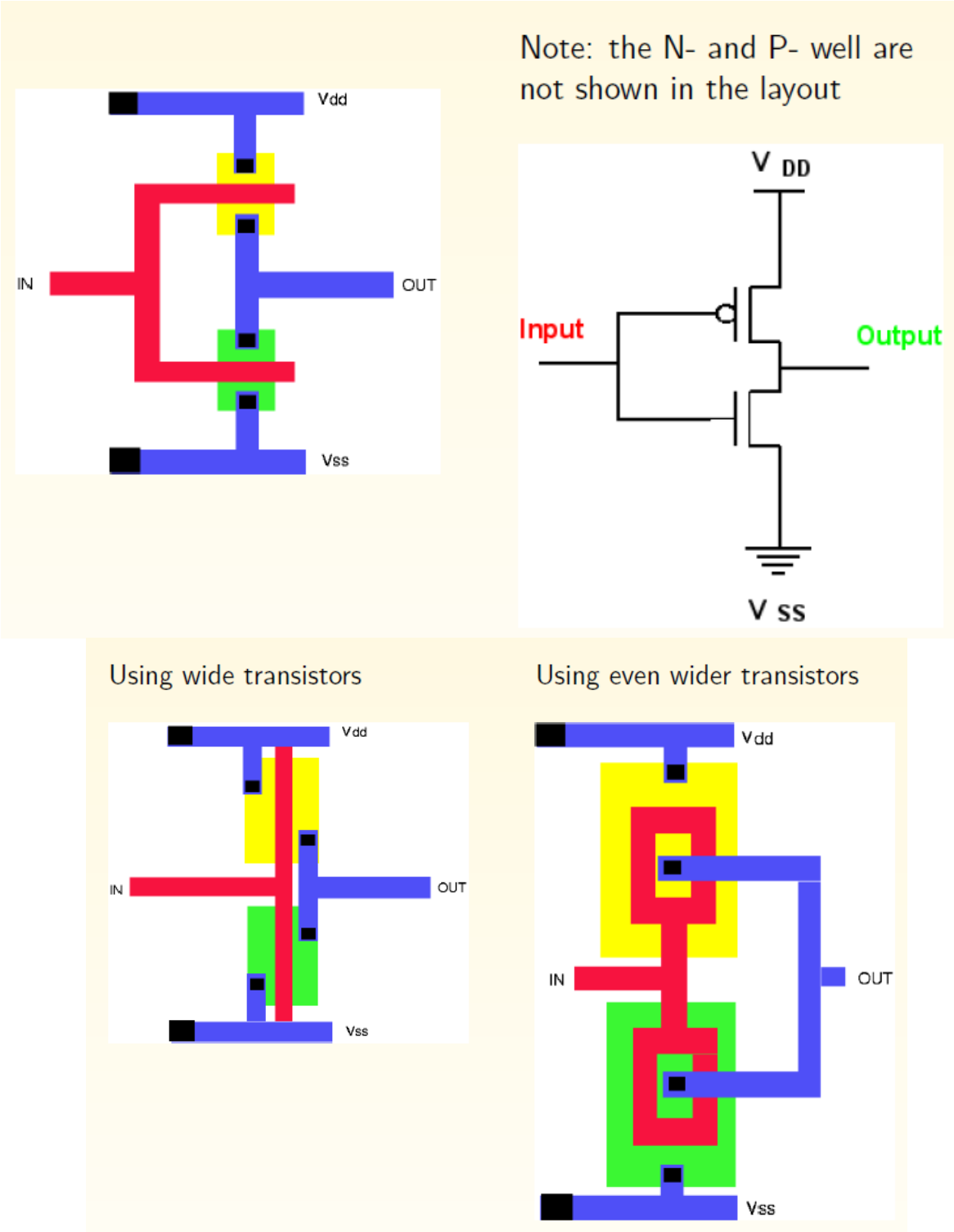


Figure: 9.4 CMOS Inverter Layout

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